CASE STUDY: A STATE-OF-THE-ART CRYOGENIC LOW-NOISE AMPLIFIER AS USED IN THE DEEP SPACE NETWORK

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Abstract

This paper presents a comprehensive study of cryogenic low-noise amplifiers (LNAs) based on GaN and GaAs technologies for applications in NASA's Deep Space Network (DSN). The work emphasizes the importance of accurate noise modeling, parameter extraction, and simulation techniques for achieving ultra-low noise performance at microwave and millimeter-wave frequencies. Various noise models, including the Pucel, Pospieszalski, Materka-Kacprzak, and Fukui approaches, are reviewed and compared with respect to their applicability in modern GaN HEMT devices. The study highlights the challenges associated with high-frequency noise parameter measurements and demonstrates the use of advanced CAD tools to predict amplifier behavior from S-parameter data. Special attention is given to temperature-dependent noise analysis, which shows that cryogenic operation significantly reduces the noise figure and improves system sensitivity. Simulation results of wideband amplifiers using both lumped and distributed elements reveal trade-offs between gain, bandwidth, and noise performance. The findings confirm that while GaN devices offer superior power handling and robustness, precise modeling and cryogenic cooling are essential to achieve optimal low-noise characteristics required for deep-space communication and radio astronomy systems.

Keywords: Cryogenic Amplifiers; GaN HEMT; Noise Modeling; Deep Space Network; Low-Noise Amplifier

1. Introduction

The Cryogenic low-noise amplifiers are used with large antennas and systems, such as the Deep Space Network. The Deep Space Network is basically the world's largest telecommunications system.

NASA describes the Deep Space Network as an "international array of giant radio antennas that supports interplanetary spacecraft missions, plus a few that orbit Earth." The DSN also facilitates radar and radio astronomy observations that are used to study the solar system and the larger universe.

The DSN consists of three complexes strategically located around the world: Goldstone (California), Madrid (Spain), and Canberra (Australia). It uses the following antenna types:

- 70-meter antennas: These are the largest and most sensitive, capable of tracking spacecraft traveling billions of miles from Earth.
- 34-meter antennas: These are also used for tracking and communication, with some being beam waveguide antennas that use a tube to guide signals to below-ground equipment rooms.
- 26-meter antennas

The DSN allows missions to perform the following functions:

- Track spacecraft
- Send commands to spacecraft
- Receive scientific data from spacecraft

The DSN is managed by NASA's Jet Propulsion Laboratory (JPL).

The highlight of this paper is the full consideration of the dynamic range of such amplifiers. This has not been done and published for this application. To accomplish this goal, special modeling software developed by Compact Software is used, as it has the necessary algorithm to correctly predict the resulting noise figures from the FET SPICE-type parameters. As to low temperature analysis, the two scientists who dominated the topic were Pucel [7] and Pospieszalski [8]. The first validation with commercial software using the Pucel approach was done by Rohde [5, 11].

Surveying existing design studies forms; the starting point of the study is reported here. In particular, the design considerations for a low-noise amplifier (LNA) discussed here are based on three papers [1-3], as well as [6] on noise mathematics and some additional references are given in the reference section [13-19].The more details on DSN can be found in [43].

A recent, comprehensive survey of microwave GaN transistor performance is found in [44]. Several high-linearity Ka-band GaN LNAs for 5 G applications have been mentioned there. As an example, a 100 nm GaN on Si LNA demonstrated a gain of $19.5-22.5$ dB from $23-30$GHz with a $0.4-1.1$ dB NF. Another work, using the same technology, reports a 26 dB gain from 33-38 GHz with a 2 dB NF. A 90 nm GaN LNA demonstrated a gain of $14.3-24.4$ dB from 18-44 GHz with a $1.5-2.5$ dB NF.

In general, the most relevant statement in this paper for the study reported here concerns accurate noise models. In particular, “A critical aspect of first-pass design success of mm-wave GaN-based LNAs is the accuracy of the noise models employed in the circuit simulators. Accurate models require precision measurements of the GaN HEMT technologies. However, as the frequency of interest increases into the mm wave range, measurement systems that can collect noise data become rare. This becomes evident when investigating the measurement and modeling of individual transistors used in GaN-based LNA designs in the literature. A 90 nm GaN HEMT was characterized and modeled across a lower $2-50$GHz frequency range and was used to project modeled performance and design the LNAs from $75-83$GHz and $91-95$GHz. A $63-101$GHz GaN-based LNA was designed using small-signal models extracted from S-parameter measurements up to 225 GHz, while the noise models were extracted from on-wafer noise parameter (NP) measurements from $8-50$GHz. It is clear from these two examples that NP measurements collected on GaN HEMT technologies in the upper mm-wave frequency ranges are rare in the literature.”

For instance, here is a Summary of mTRL (Multiline-Thru- Reflect-Line) Calibrated Noise-Parameters and Gain at **30 GHz** with **150 mA/mm** Quiescent Drain Current shown in Table 1.

Table 1. mTRL Calibrated Noise-Parameters and Gain at **30 GHz.**

W_G	L_G	V_{GS}	V_{DS}	$\mathrm{NF}_{\min}$	R_n	$\Gamma_{\mathrm{s,opt}}$	G_{assoc}
(μm)	(nm)	(V)	(V)	(dB)	(Ω)		(dB)
2×25	90	-2.07	4.0	0.61	31.6	$0.79\angle 32.5°$	10.37

Going beyond these parameters requires detailed modeling. In this paper, as it addresses low power and low noise applications, we generated from the measured S parameters linear equivalent parameters, and used S parameter transformation.

To obtain the input series, the transformation to Z11 is useful. For Z11, since the output is open, Cgd adds a few percent error. Second, from Y22 we can get rds from Re(y22), in an analog to the output capacitance. The transit frequency can be determined from

$$f_t=\frac{g_{m0}}{2\pi C_{gs}}$$

The first part of this paper provides a refresher of the methods for a detailed derivation that predicts the noise figure using noise correlation mathematics. We begin by reminding the reader of the GaAs state of the art from around the year 2000. That transistor simulation, operated at 300 K, results in a noise figure F_{min} of 1.6 dB. The paper [44] predicts a NF of around 1 dB.

In addition to GaAs, GaN devices possess useful qualities. A MESFET (Metal-Semiconductor Field-Effect Transistor) is a high-speed semiconductor device, typically made from gallium arsenide (GaAs) that uses a Schottky (metal-semiconductor) junction for its gate rather than a p-n junction. It controls electron flow by modulating the depletion layer width beneath the gate, offering superior high-frequency performance (up to 500 GHz).

The HEMT is a variation of the MESFET. Also called a heterostructure FET (HFET) or modulation-doped FET (MODFET), it is usually made with GaAs or GaN with extra layers and a Schottky junction. Depletion mode is the most common configuration. The pseudomorph or pHEMT version improves performance by using extra layers of indium to further speed electron movement.

If we take the most advanced GaN low noise transistor information and apply this to a simulated test circuit, as shown in the figure 1 below.

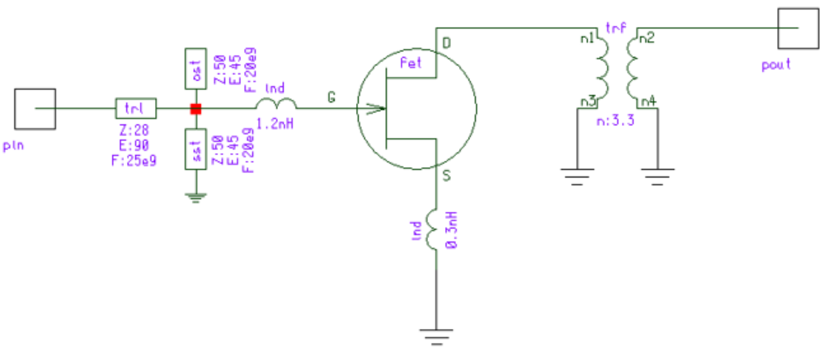

Figure 1: Linear GaN low noise amplifier.

The resulting gain prediction is more in line with the states of the art as is the predicted noise figure

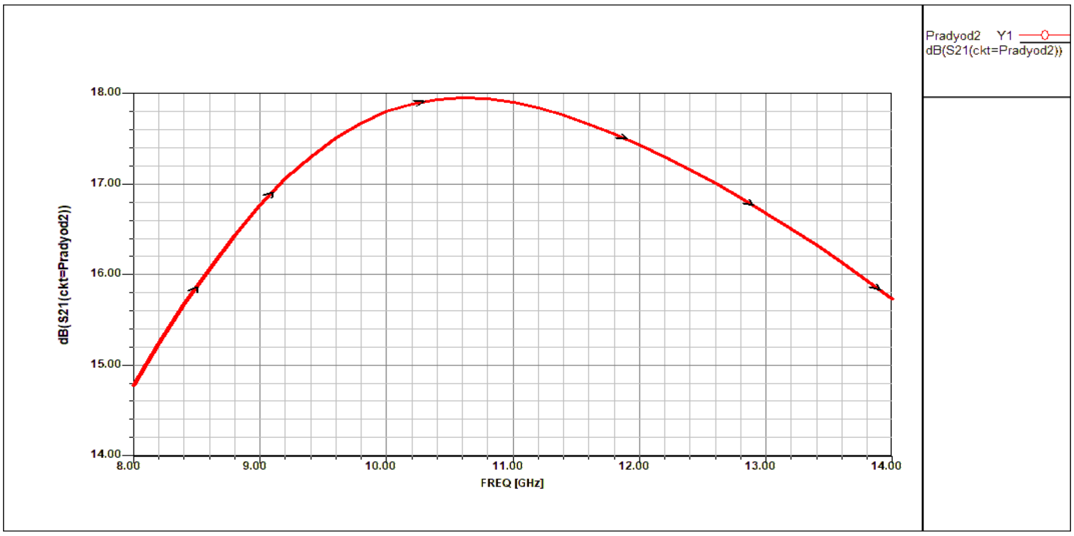

Figure 2: Simulated gain of the circuit shown in Figure 1.

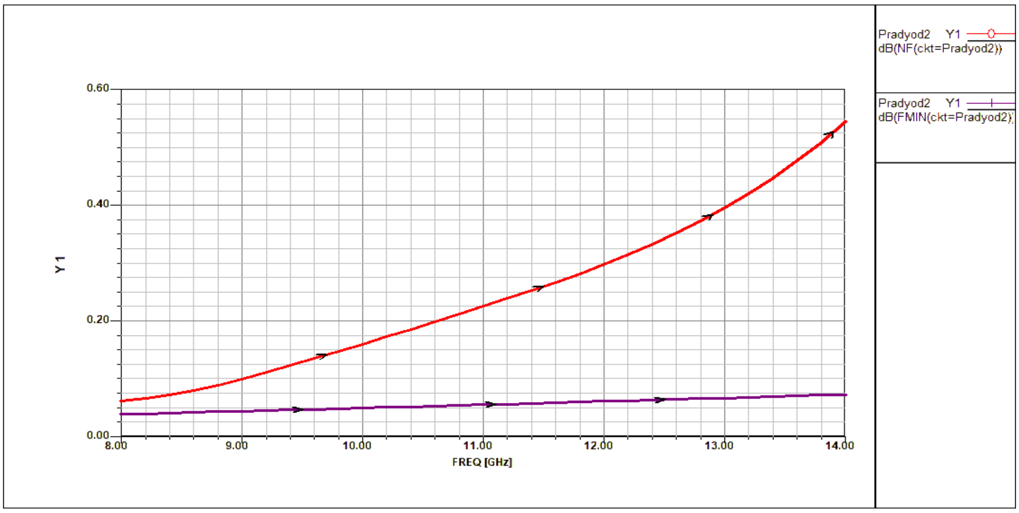

Figure 3: Simulated minimum noise figure F_{min} and NF of the circuit shown in Figure 1.

We refer the reader to some useful history about the early days of microwave circuit design, contained in [45], a classic work in high-frequency technology. It covers fundamental theories and circuits required for the use of transistors in the GHz range and is considered a pioneering work in this field. Most of the important contribution to microwave technology during 1999 are summarized in [46].

2. The GaAs-FET Noise Model and Its Application in Low-Noise Amplifiers

2.1 Linear Empirical GaAs Model

The linear model shown in Figure 4, standard in GaAs device analysis, is still successfully used as the parameter extraction is easy and it is valid for most small-signal operation.

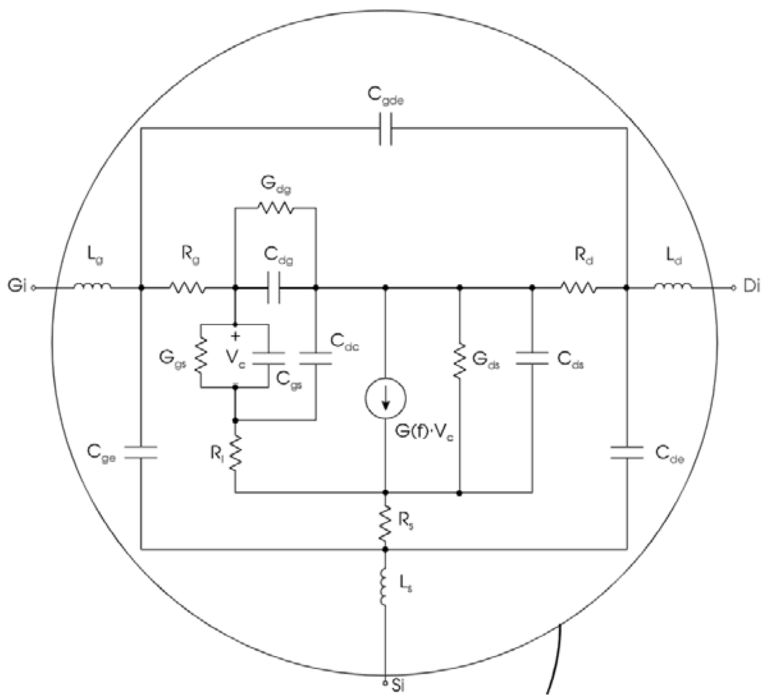

Figure 4: Linear empirical GaAs model

First, we consider MESFET devices. Noise in a MESFET is produced by sources that are intrinsic to the device. The equivalent noise circuit of an intrinsic FET is represented in Figure 5.

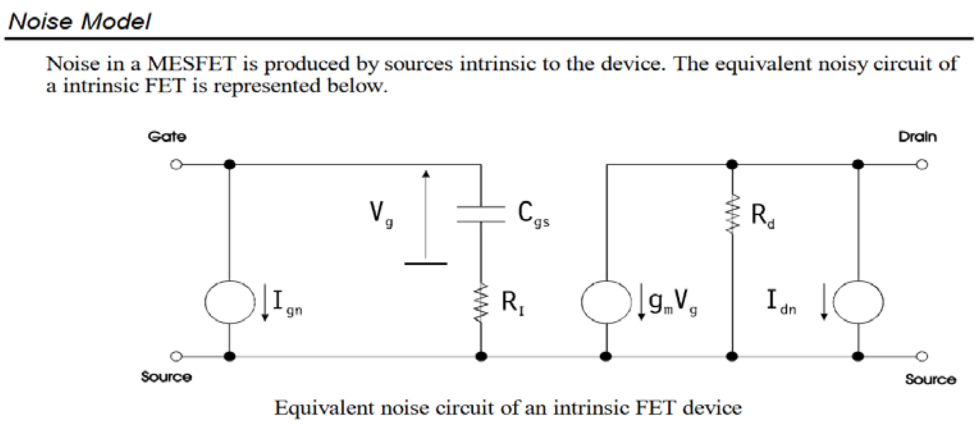

Figure 5: Equivalent simple noise circuit of an intrinsic FET device

To proceed, the Pucel model [7] is a useful approach. The following is a review of the complete derivation of the Pucel model.

The intrinsic FET is internally represented as a noiseless nonlinear two-port with one equivalent noise current source connected across the gate-source terminal, and one across the drain-source terminal. The correlations of the gate and drain noise current sources are:

$$\left\langle |I_{gn}|^2 \right\rangle = 4K_B T \Delta f \frac{\omega^2 C_{gs}^2}{g_m} R$$
$$\langle |I_{dn}|^2 \rangle = 4K_B T \Delta f g_m P \tag{1}$$
$$\left\langle I_{gn} I_{dn}^* \right\rangle = 4K_B T \Delta f j\omega C_{gs} \sqrt{PR} C$$

The correlation matrix of the noise current sources is therefore

$$C_{dc}(\omega) = \frac{2}{\pi} K_B T d\omega \begin{bmatrix} \frac{\omega^2 C_{gs}^2}{g_m} R & -j\omega C_{gs}\sqrt{PR}C \\ j\omega C_{gs}\sqrt{PR}C & g_m P \end{bmatrix} \tag{2}$$

In this model, the gate and drain noise parameters R and P, and the correlation coefficient C, are related to the physical noise sources acting in the channel and are functions of the device structure and bias point. These noise parameters at a bias point can be explicitly calculated from measured device noise parameters. By defining measured noise parameters, Fmin, Rn, and Gopt, and using a noise deembedding procedure, the parameters R, P, and C, along with the intrinsic noise correlation matrix of a FET device as functions of device bias, are determined by the modeling program that is used. In small signal cases this model also works well for GaN transistors. The concept of the R, P and C coefficient was developed by Robert Pucel from Raytheon during the MMIC DARPA program (a Raytheon-TI joint venture).

Today for large signal application and GaN devices, more modern models beyond the Pucel approach are considered. However, these have significant challenges in the parameter extraction procedure.

Flicker Noise modeling

Furthermore, in addition to the noise source models shown above, flicker (1/f) noise is present and can also be modeled by means of a noise current source connected in parallel with the intrinsic drain port. The flicker noise component in a narrow band Δf is expressed in the form

$$\left\langle |I_f|^2 \right\rangle = Q \Delta f \frac{|I_D|^{\mathrm{AF}}}{f^{\mathrm{FCP}}} \tag{3}$$

where I_D is the instantaneous value of the channel current, and Q, AF and FCP are empirical parameters. In most practical cases, AF and FCP are directly obtained from measurements (typically $\mathrm{AF} = 2, \mathrm{FCP} = 1$), while Q is not. Q is either provided directly using KF or is computed by providing the flicker corner frequency FC. FC is the frequency for which the flicker noise equals the shot/diffusion noise. The corner frequency is defined by the equation

$$Q \frac{|I_D|^{\mathrm{AF}}}{f_{\mathrm{C}}^{\mathrm{FCP}}} = g_m P \tag{4}$$

Given the corner frequency FC and the measurement bias point Vgs and Vds, analysis programs following this formulation can automatically compute required output parameters $I_D, g_{m,}$ and P, and finally Q.

2.2 General Notes on the Models

The following are some of the more popular non-linear FET-GaAs MESFET and HEMT models from the past:

- Chalmers (Angelov) Model
- Modified Materka-Kacprzak Model
- Physics-Based MESFET Models
- Pospieszalski Model

- Raytheon (Statz) Model

Note that the modified Angelov and advanced physics-based models are now dominant in modern applications.

- Raytheon (Statz) Model

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For effective noise modeling which is the subject of this paper, the models listed above have varied but substantial challenges. The Chalmers (Angelov) is a tricky hybrid model which partially calculates in the time domain and in the frequency domain. Ultimately, the CAD Tool Company may deviate from the recommended configuration as most of these models are not optimized for noise calculations. The same applies for physics based models which would need the use of the noise correlation matrix. This implies a procedure that would switch to the frequency domain calculation, obtain the 4-noise parameters (**F_{min}** (Minimum Noise Figure); **Γ_{opt}** (Optimum Source Reflection Coefficient, a complex number with magnitude & phase); and **r_n** (Equivalent Noise Resistance) and then proceed. That would not be trivial, and as most applications are toward power amplifier use this topic is usually neglected.

2.3 The Materka Model

The Materka model, developed during the time when MMICs were created, was optimized for noise calculation, and the Raytheon model is a derivative of it. This model is based on [47].

For these approaches, results critically depend on the implementation and the accuracy of the extracted parameters, and yielding correct results requires much experience and accuracy, especially when dealing with a large parameter set. Here is an example of the Materka Model spice parameters for the CFY 65 FET is shown in Figure 6.

CLY65A: GaAs-FET (HEMT), $\mathrm{Vd} = 5\ \mathrm{V}$, $\mathrm{Idss} - 70\ \mathrm{mA}$
$\mathrm{Up} < -2{,}5\ \mathrm{V}, \mathrm{Gp} > 10\ \mathrm{dB}, \mathrm{F} < 1{,}4\ \mathrm{dB}(12\mathrm{GHz})$

```
! FET DEVICE MODEL
! ACTIVE_MODEL_LIBRARY
! Manufacturer: Siemens
! NonLinear equivalent model
! File name: CFY65B.Lib
! Parameter extraction for the Materka model
! FPRINT_NAME DEVLIB4_MICROX
! Version 1.0
! DATABEGIN


.MODEL CFY65B FET (
+   IDSS=  .5919E-01  VP0 = -.1309E+01  GAMA= -.9287E-01  E    =  .5409E+00
+   KE   = -.1290E+01  SL   =  .1020E+00  KG   = -.3988E+00  T    = .4334E-12
+   SS   =  .1000E-05  IG0 =  .9746E-10  AFAG=  .2564E+02  IB0 =  .1000E-14
+   AFAB=  .2489E+02  VBC =  .8500E+01  R10 =  .5775E+01  KR   =  .0000E+00
+   C10 =  .4054E-12  K1   =  .1814E+01  C1S =  .1000E-14  CF0 =  .3923E-12
+   KF   =  .1663E+02  RG   = -.4421E+00  RD   =  .1102E+01  RS   =  .2010E+01
+   LG   =  .1134E-09  LD   =  .2170E-09  LS   =  .1492E-09  CDS =  .1118E-12
+   CDSD=  .1000E-08  RDSD=  .4983E+04  CGE =  .1000E-14  CDE =  .1000E-14
+   CGSP=  .2484E-13  CDSP=  .1876E-13  ZGT =  .6050E+02  LGT =  .1125E-02
+   ZDT =  .6050E+02  LDT =  .1125E-02  VDMX=8)
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Figure 6: The Spice parameter data of CFY 65

Figure 7 shows the Materka-Kacprazak Intrinsic Model has both intrinsic and extrinsic parameters which we will describe below in Table 2 and 3 respectively.

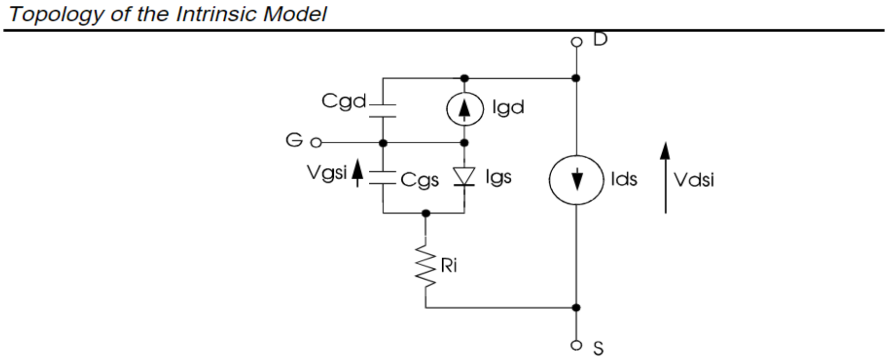

Figure 7: The Materka-Kacprazak Intrinsic Model

Table 2. Keywords of Materka-Kacprazak Intrinsic Model has both intrinsic and extrinsic parameters

keyword	description	unit	default
RG	Gate bulk and ohmic resistance	ohm	0.0
RD	Drain bulk and ohmic resistance	ohm	0.0
RS	Source bulk and ohmic resistance	ohm	0.0
LG	Gate lead inductance (metallization)	henry	0.0
LD	Drain lead inductance (metallization)	henry	0.0
LS	Source lead inductance (via)	henry	0.0
CDS	Drain-source capacitance	farad	0.0
CDSD	Low frequency trapping capacitor	farad	0.0
RDSD	Channel trapping resistance	ohm	inf
CGE	Gate-source electrode capacitance	farad	0.0
CDE	Drain-source electrode capacitance	farad	0.0
CGDE	Gate-drain electrode capacitance	farad	0.0
LGB	Gate wire bond inductance	henry	0.0
LDB	Drain wire bond inductance	henry	0.0
LSB	Source wire bond inductance	henry	0.0
CGSB	Gate bond pad to source capacitance	farad	0.0
CDSB	Drain bond pad to source capacitance	farad	0.0

CGSP	Gate to source package capacitance	farad	0.0
CDSP	Drain to source package capacitance	farad	0.0
CGDP	Gate to drain package capacitance	farad	0.0
ZGT	Gate transmission line impedance	ohm	50
ZDT	Drain transmission line impedance	ohm	50
ZST	Source transmission line impedance	ohm	50
LGT	Gate transmission line length for $\varepsilon_r = 1$	meter	0.0
LDT	Drain transmission line length for $\varepsilon_r = 1$	meter	0.0
LST	Source transmission line length for $\varepsilon_r = 1$	meter	0.0

Table 3. Channel Current Model Keywords

keywords	description	unit	default
IDSS	Drain saturation current for Vgs=0	amp	0.1
VP0	Pinch-off voltage for Vds=0	volt	-2.0
GAMA	Voltage slope parameter of pinch-off voltage	/volt	0.0
E	Constant part of power law parameter		2.0
KE	Dependence of power law on Vgs	/volt	0.0
SL	Slope of the Vgs=0 drain characteristic in the linear region	amp/volt	0.15
KG	Drain dependence on Vgs in the linear region	/volt	0.0
SS	Slope of the drain characteristic in the saturated region	amp/volt	0.0
T	Channel transit-time delay	sec	0.0
DLVL	Select diode breakdown model (default = diode model)		1
IG0	Diode saturation current	amp	0
AFAG	Slope factor of forward diode current	/volt	38.696
IB0	Breakdown saturation current	amp	0
AFAB	Slope factor of breakdown current	/volt	0
VBC	Breakdown voltage	volt	inf.
DLVL	Select Raytheon enhanced breakdown model by setting DLVL=2		
GMAX	Breakdown conductance	amp/volt	0
K1D	Fitting parameter	/volt	0

This representation contains many parameters, but we will highlight several important values.

- The channel current, Ids, is the most significant nonlinearity of the MESFET models when operating in the nominal active region. Through the first-order derivatives, Ids gives rise to the transconductance and output conductance associated with small-signal models. Higher-order derivatives produce the harmonic components and intermodulation products in the simulations.

- The capacitances, Cgs and Cgd, represent the Schottky junction capacitance of the gate-channel interface. Cds represents the stray capacitance through the substrate.
- The series resistor-capacitor pair of Rdsd-Cdsd between the intrinsic drain and source serves the purpose of increasing the output conductance of the MESFET at high frequencies. It is known that a MESFET exhibits trapping effects starting at frequencies between 10 kHz and 100 kHz which increase the output conductance. Since the equivalent output conductance of the nonlinear current source Ids is typically calculated from DC *I–V* data, the dispersion of the output conductance is not included in Ids. The Rdsd–Cdsd pair modifies the output conductance to the first order.
- The resistors R_g, R_d and R_s represent the gate metallization resistance and ohmic resistances of the drain and source contacts.
- The extrinsic parameters L_g, L_d, L_s, C_{ge}, C_{de} and C_{gde} are generally used to model wire-bond and lead inductances and inter-electrode capacitances. These parasitics are often neglected for low frequency work.
- The parameters Cgsb and Cdsb are used to model bond-pad capacitances.
- The parameters Lgb, Kdb, Lsb model wire-bond inductances of the package, while Zgt, Lgt, Zdt, Ldt, Zst, Lst model package transmission-line effects and Cgsp, Cdsp, Cgdp model package capacitances.
- The GaAs FET models have been implemented for use in the normal operating region (Vds $> \mathbf{0}$) and in the reverse operating region (Vds $< \mathbf{0}$). The normal operating region uses Vgs and Vds as the controlling voltages. The reverse operating region uses Vgd and –Vds as the controlling voltages. The equations given for the models are in the normal region.
- Lately, using foundries, the exact data about the models and their I-parameters are no longer fully disclosed, increasing the challenge of producing accurate numerical models which can predict performance..

In building an amplifier during this study, we make use of the modified Raytheon–Materka-Kacprzak model for low signals applications or where applicable. For more information, consult the references on linear operation [9-12].

2.4 GaAs Pucel FET Model at Room Temperature

We return now to the Pucel model approach in detail. Figure 8 & 9 show a noise model of a grounded source FET with noise source at input and the output. See the separate references at the end of this chapter.

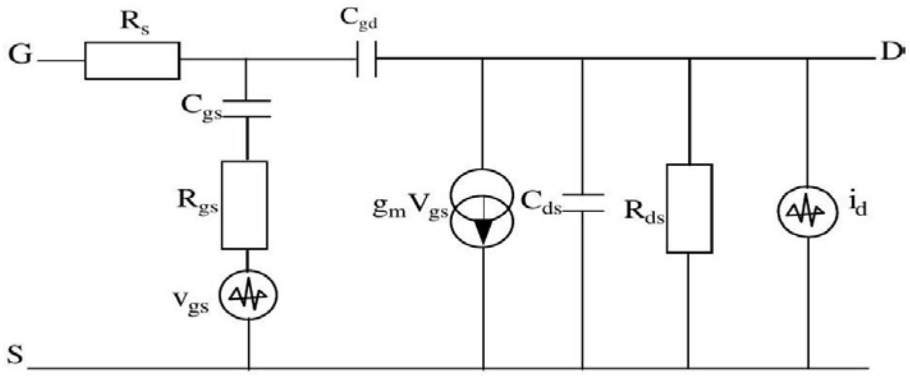

Figure 8: Noise model of a FET with voltage-noise source at input and the current-noise source at the output

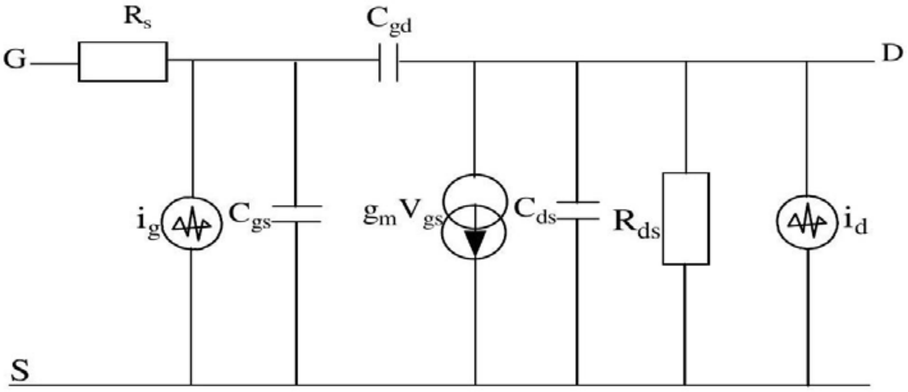

Figure 9: Noise model of a FET with current-noise source at the input and the output

The mean square value of the noise sources in the narrow frequency range Δf are given by

$$\overline{i_d^2} = 4kTg_m P\Delta f \tag{5}$$

$$\overline{i_g^2} = \frac{4kT(\omega C_{gs})^2 R}{g_m}\Delta f \tag{6}$$

$$\overline{i_g i_d^{\bullet}} = -j\omega C_{gs} 4kTC\sqrt{PR}\Delta f \tag{7}$$

$$S(i_d) = \frac{\overline{i_d^2}}{\Delta f} = \left\langle \left| \overline{i_d^2} \right| \right\rangle = 4kTg_m P \tag{8}$$

$$S(i_g) = \frac{\overline{i_g^2}}{\Delta f} = \left\langle \left| \overline{i_g^2} \right| \right\rangle = \frac{4kT(\omega C_{gs})^2 R}{g_m} \tag{9}$$

$$S(i_g i_d^{\bullet}) = \left\langle \left| \overline{i_g i_d^{\bullet}} \right| \right\rangle = -j\omega C_{gs} 4kTC\sqrt{PR} \tag{10}$$

where *P*, *R* and *C* are FET noise coefficients and are defined as

$$P = \left[\frac{1}{4kTg_m}\right]\overline{i_d^2} / Hz$$; *P* = 0.67 for JFETs and 1.2 for MESFETs (11)

$$R = \left[\frac{g_m}{4kT\omega^2 C_{gs}{}^2}\right]\overline{i_g^2} / Hz$$; *R* = 0.2 for JFETs and 0.4 for MESFETs (12)

$$C = -j\left[\frac{\overline{i_g i_d^{\bullet}}}{\sqrt{[\overline{i_d^2}\,\overline{i_g^2}]}}\right]$$; *C* =0.4 for JFETs and 0.6-0.9 for MESFETs (13)

2.5 Calculation of Noise Parameters for the Pucel Model

Figure 10 and 11 show a modified form intrinsic FET model, with noise sources at the input and output.

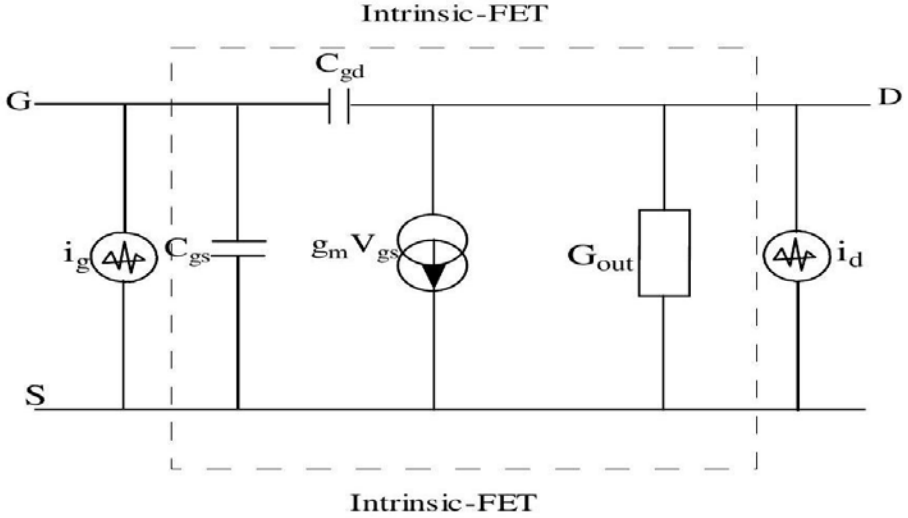

Figure 10: Intrinsic FET with noise sources at input and output

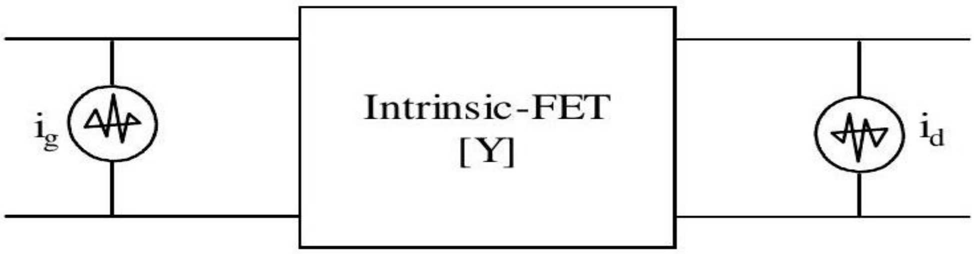

Figure 11: Intrinsic FET with noise sources at input and output

These models have expressions given as

$$[Y]_{FET-Intrinsic} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{14}$$

$$[C_Y] = [N]_{noise-matrix} = \begin{bmatrix} \overline{i_g i_g^{\bullet}} & \overline{i_g i_d^{\bullet}} \\ \overline{i_d i_g^{\bullet}} & \overline{i_d i_d^{\bullet}} \end{bmatrix} \tag{15a}$$

$$[C_Y]_{FET} = 4kT \begin{bmatrix} \frac{\omega^2 C_{gs}^2 R}{g_m} & -j\omega C_{gs} C\sqrt{PR} \\ j\omega C_{gs} C\sqrt{PR} & g_m P \end{bmatrix} \tag{15b}$$

The noise transformation from the output to input can now be done to calculate the noise parameters as follows in great detail.

Figure 12 shows the equivalent circuit of a FET with the noise source transferred to the input side.

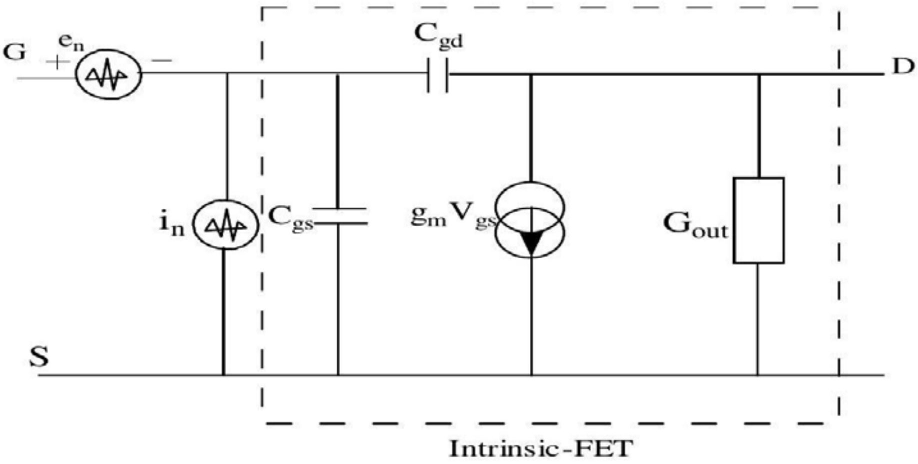

Figure 12: Equivalent circuit representation of FET with noise sources at input

From Figure 12, the ABCD parameter representation of a FET with input resistance R_S is given by

$$[ABCD]_{FET} = \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \left(\frac{sC_{gd}}{sC_{gd}-g_m}\right) & \left(\frac{1}{sC_{gd}-g_m}\right) \\ \left(\frac{sC_{gd}(g_m+g_{ds}+sC_{gs}+Ss_{ds})}{sC_{gd}-g_m}\right) & \left(\frac{sC_{gd}+g_{ds}+sC_{gs}+sC_{ds}}{sC_{gd}-g_m}\right) \end{bmatrix} \tag{16}$$

From equation 16

$$[ABCD]_{FET} = \begin{bmatrix} \left(\frac{sc_{gd}}{sc_{gd}-g_m} + \frac{R_s sc_{gd}(g_m+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) & \left(\frac{1}{sc_{gd}-g_m} + \frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) \\ \left(\frac{sc_{gd}(g_m+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) & \left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) \end{bmatrix} \tag{16a}$$

This can be rewritten as

$$\left[C_Y\right]_{FET} = 4kT \begin{bmatrix} \frac{\omega^2 c_{gs}^2 R}{g_m} & -j\omega c_{gs} C\sqrt{PR} \\ j\omega c_{gs} C\sqrt{PR} & g_m P \end{bmatrix} \tag{17}$$

$$\left[C_a\right]_{FET} = [T]\ \left[C_Y\right]_{tr} [T]^+ \tag{18}$$

$$\left[C_a\right]_{FET} = \begin{bmatrix} 0 & \left(\frac{1}{sc_{gd}-g_m} + \frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) \\ 1 & \left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) \end{bmatrix} * 4kT \begin{bmatrix} \frac{\omega^2 c_{gs}^2 R}{g_m} & -j\omega c_{gs} C\sqrt{PR} \\ j\omega c_{gs} C\sqrt{PR} & g_m P \end{bmatrix} * K1 \tag{19}$$

where;

$$K1 = \begin{bmatrix} 0 & 1 \\ \left(\frac{1}{sc_{gd}-g_m} + \frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet} & \left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet} \end{bmatrix} \tag{20}$$

$$
= 4kT\begin{bmatrix} \left(\frac{sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m}+\frac{sc_{gs}R_sC\sqrt{PR}(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) & \left(\frac{g_mP}{sc_{gd}-g_m}+\frac{g_mPR_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right) \\ \left(\frac{\omega^2c_{gs}^2R}{g_m}+\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m}\right) & \left(-j\omega c_{gs}C\sqrt{PR}+\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})g_mP}{sc_{gd}-g_m}\right) \end{bmatrix} * K2 \tag{21}
$$

where;

$$
K2 = \begin{bmatrix} 0 & 1 \\ \left(\frac{1}{sc_{gd}-g_m}+\frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet} & \left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet} \end{bmatrix} \tag{22}
$$

And reminding the reader that the usual $s = j\omega$ applies.

We then represent (21) as

$$
[C_a]_{FET} = \begin{bmatrix} C_{uu^{\bullet}} & C_{ui^{\bullet}} \\ C_{u^{\bullet}i} & C_{ii^{\bullet}} \end{bmatrix} = 4kT\begin{bmatrix} R_n & \frac{F_{\min}-1}{2}-R_nY_{opt}^{\bullet} \\ \frac{F_{\min}-1}{2}-R_nY_{opt} & R_n\left|Y_{opt}\right|^2 \end{bmatrix} \tag{23}
$$

Comparing to equations (20) and (21), the four terms of the matrix after fully resolving (21) are

$$
C_{uu^{\bullet}} = 4kT\left[\left(\frac{g_mP}{sc_{gd}-g_m}+\frac{g_mPR_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)\left(\frac{1}{sc_{gd}-g_m}+\frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet}\right] \tag{24}
$$

$$
C_{ui^{\bullet}} = 4kT\left[\left(\frac{sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m}+\frac{sc_{gs}R_sC\sqrt{PR}(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)\right] + A1 \tag{25}
$$

$$
A1 = \left[\left(\frac{g_mP}{sc_{gd}-g_m}+\frac{g_mPR_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)\left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet}\right] \tag{26}
$$

$$
C_{u^{\bullet}i} = 4kT\left[\left(-j\omega c_{gs}C\sqrt{PR}+\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})g_mP}{sc_{gd}-g_m}\right)\left(\frac{1}{sc_{gd}-g_m}+\frac{R_s(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet}\right] \tag{27}
$$

$$
C_{ii^{\bullet}} = 4kT\left[\left(\frac{\omega^2c_{gs}^2R}{g_m}+\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})sc_{gs}C\sqrt{PR}}{sc_{gd}-g_m}\right)+B1\right] \tag{28}
$$

And

$$
B1 = \left(-j\omega c_{gs}C\sqrt{PR}+\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})g_mP}{sc_{gd}-g_m}\right)\left(\frac{(sc_{gd}+g_{ds}+sc_{gs}+sc_{ds})}{sc_{gd}-g_m}\right)^{\bullet} \tag{29}
$$

and after substituting the values of $C_{uu^{\bullet}}$, $C_{ui^{\bullet}}$, $C_{u^{\bullet}i}$, $C_{ii^{\bullet}}$, we obtain the noise parameters from the right hand side of (23) as follows:

$$R_n = \frac{C_{uu^{\bullet}}}{4kT} \tag{30}$$

$$F_{\min} = \left[1 + \frac{C_{ui^{\bullet}} + C_{uu^{\bullet}} . Y_{opt}}{kT}\right] \tag{31}$$

$$Y_{opt} = \sqrt{\frac{C_{ii^{\bullet}}}{C_{uu^{\bullet}}} - \left[\mathrm{Im}\left(\frac{C_{ui^{\bullet}}}{C_{uu^{\bullet}}}\right)\right]^2} + j\,\mathrm{Im}\left(\frac{C_{ui^{\bullet}}}{C_{uu^{\bullet}}}\right) \tag{32}$$

$$Y_{opt} = G_{opt} + jB_{opt} \tag{33}$$

$$\Gamma_{opt} = \frac{\frac{1}{Y_{opt}} - \frac{1}{Y_0}}{\frac{1}{Y_{opt}} + \frac{1}{Y_0}} = \frac{Y_0 - Y_{opt}}{Y_0 + Y_{opt}} \tag{34}$$

Finally, we obtain the familiar equation as follows:

$$F = F_{\min} + \frac{R_n}{G_g}[(G_{opt} - G_g)^2 + (B_{opt} - B_G)^2] \tag{35}$$

This is the actual resulting noise figure. While amplifiers are traditionally matched for S11 and S22 complex conjugate, here at the input we need to tune for Gopt (noise matching), which may result in less power gain.

Further model simplification

Neglecting the effect of gate leakage current I_{gd} and the gate to drain capacitance C_{gd}, the models above may be further simplified, as we will demonstrate below.

Figure 13 shows the equivalent configuration of the FET without gate-drain capacitance.

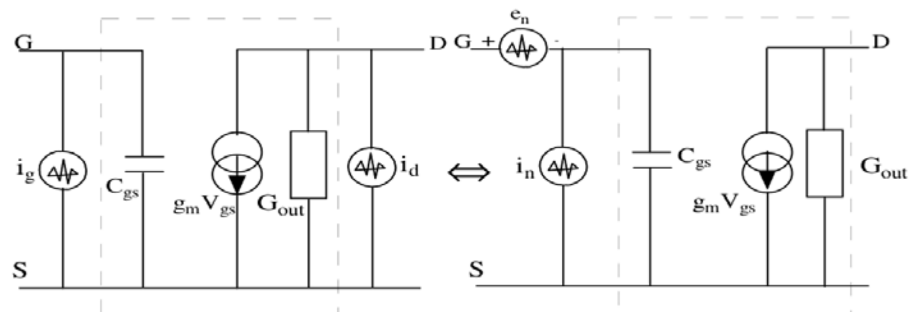

Figure 13: Equivalent configuration of the FET without gate-drain capacitance.

$$[C_a]_{tr} = \begin{bmatrix} \overline{e_n e_n^{\bullet}} & \overline{e_n i_n^{\bullet}} \\ \overline{i_n e_n^{\bullet}} & \overline{i_n i_n^{\bullet}} \end{bmatrix} \tag{36}$$

Equivalently,

$$[C_a]_{FET} = [T]\ [C_Y]_{FET}[T]^{+} \tag{37}$$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix}_{FET} \tag{38}$$

therefore

$$[C_a]_{FET} = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} [C_Y]_{FET} \begin{bmatrix} 0 & 1 \\ B_{CS}^{\bullet} & D_{CS}^{\bullet} \end{bmatrix} \tag{39}$$

The transformation matrix *T* comes from the ABCD matrix of the intrinsic FET (Figure 13).

$$[Y]_{FET} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} sc_{gs} & 0 \\ g_m & G_{out} \end{bmatrix} \tag{40}$$

$$[ABCD]_{FET} = \begin{bmatrix} A_{CS} & B_{CS} \\ C_{CS} & D_{CS} \end{bmatrix} = \begin{bmatrix} -\dfrac{y_{22}}{y_{11}} & \dfrac{1}{-y_{21}} \\ \dfrac{\Delta}{y_{21}} & \dfrac{-y_{11}}{y_{21}} \end{bmatrix} = \begin{bmatrix} -\dfrac{G_{out}}{g_m} & \dfrac{-1}{g_m} \\ \dfrac{sc_{gs}G_{out}}{g_m} & \dfrac{-sc_{gs}}{g_m} \end{bmatrix} \tag{41}$$

where; $\Delta = y_{11}y_{22} - y_{12}y_{21}$

$$[T] = \begin{bmatrix} 0 & B_{CS} \\ 1 & D_{CS} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-1}{g_m} \\ 1 & \dfrac{-sc_{gs}}{g_m} \end{bmatrix} \tag{42}$$

Where T's complex transpose is therefore

$$[T]^{+} = \begin{bmatrix} 0 & 1 \\ B_{CS}^{\bullet} & D_{CS}^{\bullet} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \tag{43}$$

and

$$[C_a]_{FET} = [T]\ [C_Y]_{FET} [T]^{+} \tag{44}$$

$$[C_a]_{FET} = \begin{bmatrix} 0 & \dfrac{1}{-g_m} \\ 1 & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} * 4kT \begin{bmatrix} \dfrac{\omega^2 c_{gs}^2 R}{g_m} & -j\omega c_{gs} C\sqrt{PR} \\ j\omega c_{gs} C\sqrt{PR} & g_m P \end{bmatrix} * \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-g_m} & \dfrac{sc_{gs}}{-g_m} \end{bmatrix} \tag{45}$$

$$[C_a]_{FET} = 4kT \begin{bmatrix} \dfrac{-j\omega C_{gs} C\sqrt{PR}}{g_m} & -P \\ \dfrac{\omega^2 C_{gs}^2 R}{g_m} + \dfrac{\omega^2 C_{gs}^2 C\sqrt{PR}}{g_m} & -j\omega C_{gs}(P + C\sqrt{PR}) \end{bmatrix} * \begin{bmatrix} 0 & 1 \\ \dfrac{-1}{g_m} & \dfrac{-SC_{gs}}{g_m} \end{bmatrix} \tag{45a}$$

Substitute $S = j\omega$ in equation (45a); from that noise correlation matrix becomes

$$[C_a]_{FET} = \frac{4kT}{g_m} \begin{bmatrix} P & j\omega C_{gs}(P - C\sqrt{PR}) \\ j\omega C_{gs}(P + C\sqrt{PR}) & \omega^2 C_{gs}^2(R - P) \end{bmatrix} \tag{46}$$

$$[C_a]_{FET} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \frac{4kT}{g_m}\begin{bmatrix} P & j\omega C_{gs}(P - C\sqrt{PR}) \\ j\omega C_{gs}(P + C\sqrt{PR}) & \omega^2 C_{gs}^2(R - P) \end{bmatrix} \tag{47}$$

From Equation (47) we obtain,

$$C_{11} = \frac{4kTP}{g_m} \qquad C_{12} = \frac{4kTj\omega C_{gs}(P - C\sqrt{PR})}{g_m} \tag{47a}$$

$$C_{21} = \frac{4kTj\omega C_{gs}(P + C\sqrt{PR})}{g_m} \qquad C_{22} = \frac{4kT\omega^2 C_{gs}^2(R - P)}{g_m} \tag{47b}$$

and after substituting the values of $\begin{matrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{matrix}$, we obtain the noise parameters as follows:

(Noise resistance R_n)

$$R_n = \frac{|C_{12}|^2}{4kTC_{11}} = \frac{\omega^2 C_{gs}^2}{Pg_m}\left(P - C\sqrt{PR}\right)^2 \tag{48}$$

$$Y_{opt} = \sqrt{\frac{C_{22}}{C_{11}}} - \frac{C_{12}}{C_{11}} = \omega C_{gs}\sqrt{\frac{(R-P)}{P}} - j\,\omega C_{gs}\frac{(P - C\sqrt{PR})}{P} \tag{49}$$

$$Y_{opt} = \frac{1}{Z_{opt}} = G_{opt} + jB_{opt} \tag{50}$$

So, if we compare Equation (49) and (50); we get

$$G_{opt} = \omega C_{gs}\sqrt{\frac{(R-P)}{P}} \quad and \quad B_{opt} = -\,\omega C_{gs}\frac{(P - C\sqrt{PR})}{P} \tag{50a}$$

From that we obtain real part R_{opt} and imaginary part X_{opt} as follows

$$optimum\,resistance\;R_{opt} = \frac{G_{opt}}{G_{opt}^2 + B_{opt}^2} = \frac{\sqrt{\frac{(R-P)}{P}}}{\omega C_{gs}\left[\frac{(R-P)}{P} - \frac{(P - C\sqrt{PR})^2}{P^2}\right]} \tag{51a}$$

$R_{opt} \approx \frac{1}{\omega C_{gs}}\sqrt{\frac{P}{R}};\; since\;|B_{opt}| \gg |G_{opt}|\; high\,frequency\,appoximation$ and

$$optimum\,reactance\;X_{opt} = \frac{\frac{(P - C\sqrt{PR})}{P}}{\omega C_{gs}\left[\frac{(R-P)}{P} - \frac{(P - C\sqrt{PR})^2}{P^2}\right]} \approx \frac{1}{\omega C_{gs}} \tag{51b}$$

Minimum Noise Figure F_{min} can be calculated as follows

$$F_{min} = 1 + \frac{1}{2kT}(C_{11} + C_{22} - 2|C_{12}|) \tag{52}$$

$$= 1 + \frac{2P}{g_m} + \frac{2\omega^2 C_{gs}^2(R-P)}{g_m} - \frac{4\omega C_{gs}(P - C\sqrt{PR})}{g_m} \tag{53}$$

Where,

$P = \left[\frac{1}{4kTg_m}\right]\overline{i_d^2}\,/\,Hz$; P = 0.67 for JFETs and 1.2 for MESFETs (54a)

$R = \left[\frac{g_m}{4kT\omega^2 C_{gs}^{\;2}}\right]\overline{i_g^2}\,/\,Hz$; R = 0.2 for JFETs and 0.4 for MESFETs (54b)

$$C = -j\left[\frac{\overline{i_g i_d^{\bullet}}}{\sqrt{[\overline{i_d^2}\,\overline{i_g^2}]}}\right]$$; C =0.4 for JFETs and 0.6-0.9 for MESFETs (54c)

This equation is valid for the somewhat simpler equivalent circuit. A more detailed noise-equivalent model and its derivation are found in [4].

2.6 Influence of Cgd, Rgs, and Rs on the Noise Parameters

We now introduce additional device parameters (Figure 13) and examine their effects on noise performance. Rewriting previous expressions,

$$[C_a]_{FET} = \begin{bmatrix} C_{uu^{\bullet}} & C_{ui^{\bullet}} \\ C_{u^{\bullet}i} & C_{ii^{\bullet}} \end{bmatrix} \tag{55}$$

$$C_{uu^{\bullet}} = \left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left(\frac{P + R - 2C_r\sqrt{PR}}{g_m}\right) + (R_s + R_{gs}) \tag{56}$$

$$C_{ui^{\bullet}} = \left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left[\left(\frac{\omega^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{j\omega c_{gd}}{g_m}\right)(R - C\sqrt{PR}) - \frac{j\omega c_{gd}}{g_m}(P - C^{\bullet}\sqrt{PR})\right] \tag{57}$$

$$C_{ii^{\bullet}} = \left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left[\left|\frac{\omega^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{j\omega c_{gd}}{g_m}\right|^2 \frac{R}{g_m} + \left|\frac{j\omega c_{gs}}{g_m}\right|^2 Pg_m\right] +$$

$$\left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left[2\,\mathrm{Re}\left\{\left(\frac{\omega^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{j\omega c_{gd}}{g_m}\right)\left(\frac{j\omega c_{gs}}{g_m}\right) C\sqrt{PR})\right\}\right] \tag{58}$$

$$C_{u^{\bullet}i} = \left\{\left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left[\left(\frac{\omega^2 C_{gs}^2 C_{gd}^2}{g_m^2} + \frac{j\omega c_{gd}}{g_m}\right)(R - C\sqrt{PR}) - \frac{j\omega c_{gd}}{g_m}(P - C^{\bullet}\sqrt{PR})\right]\right\}^{\bullet} \tag{59}$$

where;

$$\frac{R}{g_m} = \overline{e_n e_n^{\bullet}} \tag{60}$$

$$Pg_m = \overline{i_n i_n^{\bullet}} \tag{61}$$

$$C = \frac{\overline{|e_n i_n^{\bullet}|}}{\sqrt{\left(\overline{e_n e_n^{\bullet}}\right)\left(\overline{i_n i_n^{\bullet}}\right)}} = \frac{\overline{|e_n i_n^{\bullet}|}}{\sqrt{|e_n^2||i_n^2|}} \tag{62}$$

$$[C_a]_{FET} = \begin{bmatrix} C_{uu^{\bullet}} & C_{ui^{\bullet}} \\ C_{u^{\bullet}i} & C_{ii^{\bullet}} \end{bmatrix} = \begin{bmatrix} R_n & \dfrac{F_{\min} - 1}{2} - R_n Y_{opt}^{\bullet} \\ \dfrac{F_{\min} - 1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \tag{63}$$

The modified expressions for the noise parameters are now:

$$R_n = C_{uu^\bullet} \tag{64}$$

$$Y_{opt} = \sqrt{\frac{C_{ii^\bullet}}{C_{uu^\bullet}} - \left[\mathrm{Im}\left(\frac{C_{ui^\bullet}}{C_{ii^\bullet}}\right)\right]^2} + j\,\mathrm{Im}\left(\frac{C_{ui^\bullet}}{C_{uu^\bullet}}\right) \tag{65}$$

$$Z_{opt} = \sqrt{\frac{C_{uu^\bullet}}{C_{ii^\bullet}} - \left(\frac{\mathrm{Im}\,C_{ui^\bullet}}{C_{ii^\bullet}}\right)^2} - j\left(\frac{\mathrm{Im}\,C_{ui^\bullet}}{C_{ii^\bullet}}\right) \tag{66}$$

$$Y_{opt} = G_{opt} + jB_{opt} \tag{67}$$

$$F_{\min} = 1 + 2\left[\mathrm{Re}(C_{ui^\bullet}) + C_{ii^\bullet}\,\mathrm{Re}(Z_{opt})\right] \tag{68}$$

$$F_{\min} = 1 + 2\left[\left(\frac{\omega^2 c_{gs}^2}{g_m^2}\right)(R_{gs} + R_s)Pg_m + \sqrt{\frac{\omega^4 c_{gs}^4}{g_m^4}(R_{gs} + R_s)^2 P^2 g_m^2 + \left(\frac{\omega^2 c_{gs}^2}{g_m^2}\right)[PR(1 - C^2) - Pg_m R_{gs}]}\right] \tag{69}$$

$$R_n = \left|\frac{g_m}{g_m - j\omega c_{gd}}\right|^2 \left(\frac{P + R - 2C_r\sqrt{RP}}{}\right) + (R_{gs} + R_s) \tag{70}$$

$$R_{opt} = \frac{1}{\omega c_{gs}}\sqrt{\frac{g_m(R_s + R_{gs}) + R(1 - C_r^2)}{P} + \omega^2 c_{gs}^2 (R_s + R_{gs})^2} \tag{71}$$

$$X_{opt} = \frac{1}{\omega c_{gs}}\left(1 - C_r\sqrt{\frac{R}{P}}\right) \tag{72}$$

In general, $F_{\min}$ is best determined with a suitable CAD tool, which will be discussed in a future publication.

2.7 FET Minimum noise factor

The noise factor of the FET, the minimum noise factor, according to Fukui [12], can be easily calculated. He reported a useful empirical method to determine the minimum noise figure (NFmin) at any temperature for a FET such as GaAs or GaN. The Fukui equation is:

$$NF_{\min} = 10\log\left\{1 + \frac{K_F F}{f_T}\left[g_m(R_g + R_s)\right]^{0.5}\right\} \tag{73}$$

where f_T is the current gain cutoff frequency, F is the frequency of operation, g_m is the transconductance, R_g and R_s are gate and source resistances, respectively, and K_F is the empirical fitting factor. As long as parasitic resistors in GaN transistors have larger values (due to technology), the GaAs FET remains the better choice from a noise point of view.

Some have used the Fukui equation to calculate the minimum noise figure of GaN HEMTs by appropriately determining an empirical fitting factor KF. For short gate-length transistors, the empirical fitting factor is recommended to be

$$K_F = 2\left(\frac{I_{opt}}{E_c L_g g_m}\right)^{0.5} \tag{74}$$

Where; I_{opt} is the optimum current for minimum noise operation, L_g is the gate length and E_c is the critical electric field.

Therefore, we get:

$$NF_{\min} = 10\log\left\{1 + \frac{2F}{f_T}\left[\frac{I_{opt}(R_g+R_s)}{E_c L_g}\right]^{0.5}\right\} \quad (75)$$

I_{opt} is about 20% of Idss, Ec is assumed 150kV/cm and Lg is the gate length [40].

2.8 Temperature Dependency of the Noise Parameters of an FET

We will now introduce a minimum noise temperature $T_{\min}$ and modify the noise parameters that were previously derived. At low temperatures, transistors experience reduced thermal noise because charge carriers have less energy, but other effects such as quantum noise, carrier freeze-out, and increased variability can significantly influence their noise performance. The impact of lower temperature on the overall noise figure are discussed in [20-39].

As pointed out in the introduction, we are motivated to perform this modification because the lowest noise factor (ultimately lowest noise figure) is needed for DSN and other weak signal applications. The Nyquist formula states

$$Pn = kTo \quad (76)$$

As we reduce To from 290 K (room temperature) to a much lower temperature like 27 K, the sensitivity will increase. We must therefore modify the FET models to have temperature dependence factors.

For cryogenic LNA applications, extremely low noise temperatures are needed. In particular, these amplifiers are cooled cryogenically to temperatures close to zero degrees kelvin (K). Since there are no direct measurements available, we must develop a strategy to predict performance without these direct measurements. The following method allows prediction of the noise performance of FETs under appropriate "cooled" conditions, and provides derivations to calculate the temperature-dependent noise performance.

Figure 14 shows the familiar two-port noise representation of the intrinsic FET in admittance (a) and ABCD matrix form (b).

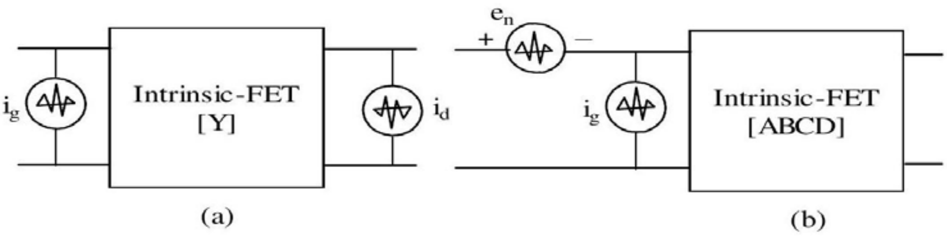

Figure 14: Noise representation in linear two-port: (a) Current noise source at input and output and (b) current and voltage noise source at input

The admittance representation of the noise parameters of the intrinsic FET is expressed as follows:

$$G_1 = \frac{\overline{|i_g^2|}}{4kT_0\Delta f} \quad (77)$$

$$G_2 = \frac{\overline{|i_d^2|}}{4kT_0\Delta f} \quad (78)$$

$$C_r = \frac{\overline{\left| i_g i_d^{\bullet} \right|}}{\sqrt{\left| i_d^2 \right| \left| i_g^2 \right|}} \tag{79}$$

where k is the Boltzmann constant ($k = 1.38 \times 10^{-23}$J/K), T_0 is standard room temperature (290 K), and Δf is the reference bandwidth in Hz.

The ABCD matrix representation and the corresponding noise parameters are as follows:

$$R_n = \frac{\overline{\left| e_n^2 \right|}}{4kT_0 \Delta f} \tag{80}$$

$$g_n = \frac{\overline{\left| i_n^2 \right|}}{4kT_0 \Delta f} \tag{81}$$

$$C_r = \frac{\overline{\left| e_n i_n^{\bullet} \right|}}{\sqrt{\left| e_n^2 \right| \left| i_n^2 \right|}} \tag{82}$$

$$N = R_{opt} g_n \tag{83}$$

Where g_n is the noise conductance.

The expression for the noise temperature T_n and a noise measure M of a two-port driven by generator impedance Z_g is expressed as follows (consistent with the previously shown equation for the actual noise factor in case of non-optimal input matching):

$$T_n = T_{\min} + T_0 \frac{g_n}{R_g} \left| Z_g - Z_{opt} \right|^2 \tag{84a}$$

$$T_n = T_{\min} + NT_0 \frac{\left| Z_g - Z_{opt} \right|^2}{R_g R_{opt}} \tag{84b}$$

$$T_n = T_{\min} + 4NT_0 \frac{\left| T_g - T_{opt} \right|^2}{(1 - \left| T_{opt} \right|^2)(1 - \left| T_g \right|^2)} \tag{84c}$$

$$T_{opt} = \frac{Z_{opt} - Z_o}{Z_{opt} + Z_o} \tag{85}$$

$$M = \frac{T_n}{T_0} \left(\frac{1}{1 - \frac{1}{G_a}} \right) \tag{86}$$

where Z_0 is the reference impedance and G_a is the available gain.

An extrinsic FET with parasitic resistances is shown in Figure 15. The parasitic elements contribute thermal noise, and their influence can be calculated based on the ambient temperature T_a. The G1 and G2 are normalized parasitics elements shown in equation 87a and 87b.

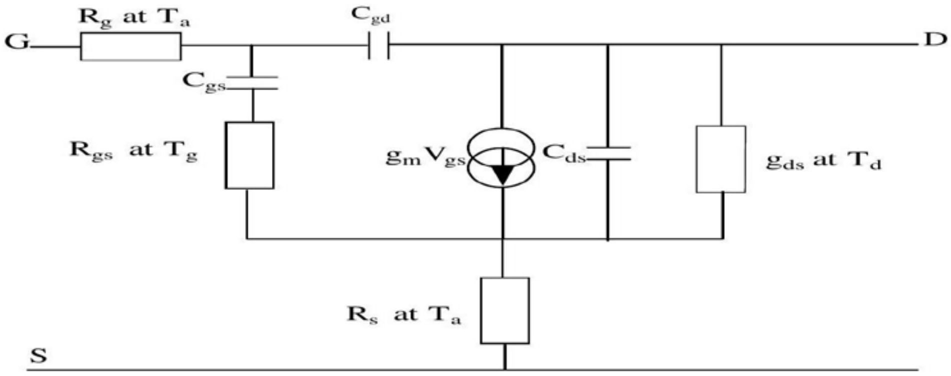

Figure 15: Extrinsic FET with parasitic resistances.

$$G_1 = \frac{T_g}{T_o} \frac{R_{gs}(\omega C_{gs})^2}{(1+\omega^2 C_{gs}^2 R_{gs}^2)} \tag{87a}$$

$$G_2 = \frac{T_g}{T_o} \frac{g_m^2 R_{gs}}{(1+\omega^2 C_{gs}^2 R_{gs}^2)} + \frac{T_d}{T_o} g_{gs} \tag{87b}$$

$$C_{r_c} = C_r \frac{\overline{\left|i_g i_d^\bullet\right|}}{\sqrt{\left|i_d^2\right|\left|i_g^2\right|}} = \frac{-j\omega g_m C_{gs} R_{gs}}{(1+\omega^2 C_{gs}^2 R_{gs}^2)} \frac{T_g}{T_o} \tag{88}$$

The noise properties of the intrinsic FET are treated by assigning an equivalent temperature gate temperature T_g and drain temperature T_d to R_{gs} and g_{ds}. No correlation is assumed between the noise sources represented by the equivalent temperature T_g and T_d shown in Figure 16.

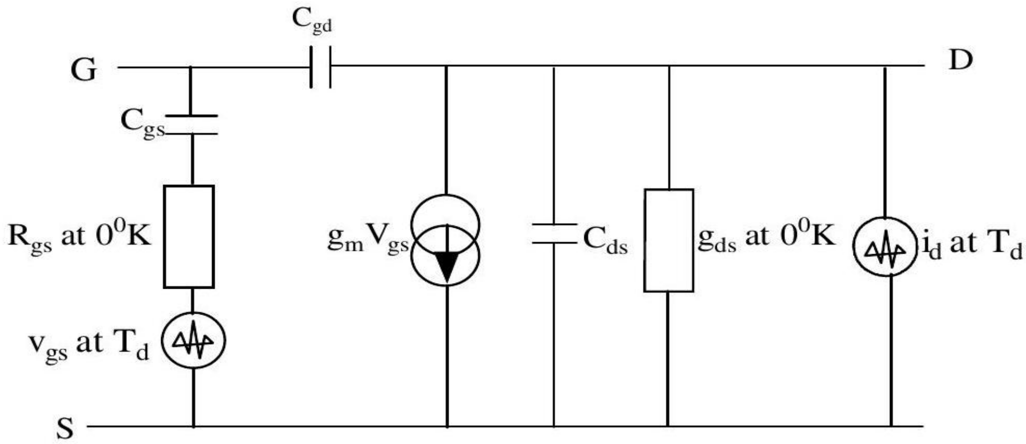

Figure 16: Intrinsic FET with assigned equivalent temperature.

The modified noise parameters are expressed as follows:

$$Z_{opt} = R_{opt} + jX_{opt} \tag{89}$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{R_{gs}}{R_{ds}}\frac{T_g}{T_d} + R_{gs}^2} \tag{90}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} \tag{91}$$

$$T_{min} = 2\frac{f}{f_T}\sqrt{R_{gs}g_{ds}T_gT_d + \left(\frac{f}{f_T}\right)^2 R_{dgs}{}^2 g_{ds}{}^2 T_d{}^2} + 2\left(\frac{f}{f_T}\right)^2 R_{gs}g_{ds}T_d \tag{92}$$

$$T_{\min} = (F_{\min} - 1)T_0 \tag{93}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}T_d}{T_0} \tag{94}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{95}$$

$$\frac{4NT_0}{T_{\min}} = \frac{2}{1 + \frac{R_{gs}}{R_{opt}}} \tag{96}$$

$$R_n = \frac{T_g}{T_o}R_{gs} + \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(1 + \omega^2 C_{gs}^2 R_{gs}^2) \tag{97}$$

$$C_r = C\sqrt{R_n g_n} = \frac{T_d}{T_0}\frac{g_{ds}}{g_m^2}(\omega^2 C_{gs}^2 R_{gs} + j\omega C_{gs}) \tag{98}$$

2.9 Noise Approximation expressions

With some reasonable approximation, the expression for the noise parameters becomes much simpler. In particular, by introducing the following approximation, the obtained values from the calculation typically vary less than 5% from the exact value.

Given the following:

$$if\ \frac{f}{f_T} \le \sqrt{\frac{R_{gs}}{R_{ds}}\frac{T_g}{T_d}} \tag{99}$$

and $R_{opt} \ge R_{gs}$, then

$$R_{opt} \cong \left(\frac{f_T}{f}\right)\sqrt{\frac{r_{gs}}{r_{ds}}\frac{T_g}{T_d}} \tag{100}$$

$$X_{opt} \cong \frac{1}{\omega C_{gs}} \tag{101}$$

$$T_{\min} \cong 2\frac{f}{f_T}\sqrt{r_{gs}g_{ds}T_gT_d} \tag{102}$$

$$g_n \cong \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}T_d}{T_0} \tag{103}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{104}$$

$$\frac{4NT_0}{T_{\min}} \cong 2 \tag{105}$$

For Example: A linear FET model with the following intrinsic parameters is assumed:

R_{gs} = 2.5 Ω C_{gd} = 0.042 pF

r_{ds} = 400 Ω g_m = 57 mS

C_{gs} = 0.28 pF f = 8.5 GHz

C_{ds}=0.067 pF

The temperature-dependent noise parameters for the intrinsic FET are now calculated for two cases (room temperature).

Example 1: T_a = 297 K, T_g = 304 K, T_d = 5514 K, V_{ds} = 2 V, Ids = 10 mA

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39GHz \tag{106}$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 28.42\Omega \tag{107}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} = 66.91\Omega \tag{108}$$

$$T_{min} = 2\frac{f}{f_T}\sqrt{R_{gs}g_{ds}T_gT_d + \left(\frac{f}{f_T}\right)^2 R_{dgs}{}^2 g_{ds}{}^2 T_d{}^2} + 2\left(\frac{f}{f_T}\right)^2 R_{gs}g_{ds}T_d = 58.7\text{K} \tag{109}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}T_d}{T_0} = 3.27\text{mS} \tag{110}$$

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{58.7}{290} + 1 = 1.59\ dB \tag{111}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds}T_d}{T_0 g_m^2}(1+\omega^2 r_{gs}^2 c_{gs}^2) = 17.27\Omega \tag{112}$$

Example 2: T_a = 12.5 K, T_g = 14.5 K, T_d = 1406 K, V_{ds} = 2 V, Ids = 5 mA (cooled down to 14.5 K)

$$f_T = \frac{g_m}{2\pi C_{gs}} = 32.39\,GHz \tag{113}$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} = 12.34\Omega \tag{114}$$

$$X_{opt} = \frac{1}{\omega C_{gs}} = 66.9\Omega \tag{115}$$

$$T_{min} = 2\frac{f}{f_T}\sqrt{R_{gs}g_{ds}T_gT_d + \left(\frac{f}{f_T}\right)^2 R_{dgs}{}^2 g_{ds}{}^2 T_d{}^2} + 2\left(\frac{f}{f_T}\right)^2 R_{gs}g_{ds}T_d = 7.4\text{K} \tag{116}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}T_d}{T_0} = 0.87\text{mS}$$
(117)

$$F_{\min} = \frac{T_{\min}}{T_0} + 1 = \frac{7.4}{290} + 1 = 0.21dB \tag{118}$$

$$R_n = \frac{T_g r_{gs}}{T_0} + \frac{g_{ds}T_d}{T_0 g_m^2}(1 + \omega^2 r_{gs}^2 c_{gs}^2) = 3.86\Omega \tag{119}$$

These results [6] are consistent with those published by Pucel [7] and Pospieszalski [8].

To summarize, the PRC model, based on the work of Pucel et al., is a current source model, where the current sources are connected to the input and output ports of the intrinsic transistor. The current sources are correlated and the correlation is imaginary. The advantages of the PRC model are its close connection to the physical processes.

The parameters P, R, and C are given below, along with the minimum noise figure, $F_{\min}$:

$$P = \frac{\langle i_d i_d^* \rangle}{4kT_0 B g_m} \tag{120a}$$

$$R = \frac{\langle i_g i_g^* \rangle g_m}{4kT_0 B (\omega C_{gs})^2} \tag{120b}$$

$$C = -j\frac{\langle i_g i_d^* \rangle}{\sqrt{\langle i_g i_g^* \rangle \langle i_d i_d^* \rangle}} \tag{120c}$$

and

$$F_{\min} = 1 + 2\sqrt{PR(1 - C^2)}\frac{f}{f_T} + 2g_m R_i P\left(1 - C\sqrt{\frac{P}{R}}\right)\left(\frac{f}{f_T}\right)^2 \tag{121}$$

Later the Cappy Model was developed (see extension to ref 7), it allows to take into account nonstationary carrier transport and to consider longitudinal fields of arbitrary shape.

2.10 The Pospieszalski Noise Model

Pospieszalski model uses small signal circuit elements that yield closed-form expressions for the noise parameters. This model introduces frequency-independent equivalent temperatures T_g and T_d for the intrinsic gate resistance $R_i(Rg)$ and drain resistance R_{ds}, respectively. The noise processes are modeled by R_{ds}, and T_d is the only free parameter, while T_g is taken to be the ambient temperature of the device. The noise correlation relations are given here:

$$R_{ds} = \frac{\langle i_d i_d^* \rangle}{4kT_d B} \text{ and } R_i = \frac{\langle i_g i_g^* \rangle}{4kT_g B} \tag{122}$$

$$\langle i_d i_d{}^* \rangle = 0$$

The noise parameters for the above intrinsic circuit are given by the following expressions

$$R_{\mathrm{opt}} = \sqrt{\frac{T_g R_i R_{ds}}{T_d}\left(\frac{g_m}{\omega C_{gs}}\right)^2 + R_i^2} \tag{123}$$

$$X_{\mathrm{opt}} = \frac{1}{\omega C_{gs}} \tag{124}$$

$$T_{\mathrm{min}} = 2\frac{\omega C_{gs}}{g_m}\sqrt{\frac{T_d T_g R_i}{R_{ds}} + \left(\frac{T_d R_i \omega C_{gs}}{R_{ds} g_m}\right)^2} + 2\frac{T_d R_i}{R_{ds}}\left(\frac{\omega C_{gs}}{g_m}\right)^2 \tag{125}$$

Please refer Table 4 for T_{min} to Fmin conversion, and

$$R_n = \frac{T_{\mathrm{min}}}{T_0} R_i + \frac{T_d}{T_0}\frac{1}{R_{ds} g_m^2}\left(1 + \left(\omega C_{gs} R_i\right)^2\right) \tag{126}$$

The utility of this model is that it allows prediction of the noise parameters for a broad frequency range from a single frequency noise-parameter measurement at a given temperature. Although the Pospieszalski model only considers thermal noise sources and does not take into account the correlated noise between the gate and the drain, it is an accurate model for high-quality devices operated at low-noise bias. Additionally, for devices operated at higher drain currents, T_g is taken to be higher than the ambient temperature; and gate leakage current can be modeled with a resistor across C_{gs} and R_i at an elevated temperature.

2.11 The Fukui Model

This most well-established model for device and circuit optimization is the semi-empirical one developed by Fukui. In the Fukui model, the noise parameters are simple frequency dependent functions of the equivalent small-signal intrinsic circuit elements (transconductance, g_m, gate-to-source capacitance, C_{gs}, and source and gate resistances, R_s and R_g). These circuit elements are (in turn) analytic functions of the device's geometrical (e.g., gate and channel dimensions) and material (e.g., doping) concentration and active channel thickness) parameters. The semi-empirical approach of Fukui yields the following expressions for the noise parameters:

$$T_{\mathrm{min}} = \frac{k_1 \omega T_0 C_{gs}}{2\pi}\sqrt{\frac{(R_g + R_s)}{g_m}} \tag{127}$$

$$R_n = \frac{k_2}{g_m} \tag{128}$$

$$R_{\mathrm{opt}} = k_3\left(\frac{1}{4 g_m} + R_g + R_s\right) \tag{129}$$

$$X_{\mathrm{opt}} = \frac{2\pi k_4}{\omega C_{gs}} \tag{130}$$

Where; k_1, k_2, k_3, and k_4 are fitting factors that are determined experimentally. This model is equivalent-circuit dependent and provides little insight into the physics of noise in HEMTs [41].

3 Experimental FET-Based Wideband Amplifier Example Simulation with Lumped Lossless Components

Figure 17 shows experimental FET-based wideband amplifier with lumped lossless components. This simulation approach, which later compares with measured and simulated data, uses a novel adjustment to the Materka Model which is proprietary. Junction temperature is 15 K as shown in figure 17 on the right lower side. The nominal temperature is 10 k; the difference is due to the thermal conductivity which should be much better to get an even lower operating noise figure. This will be an important topic throughout the paper.

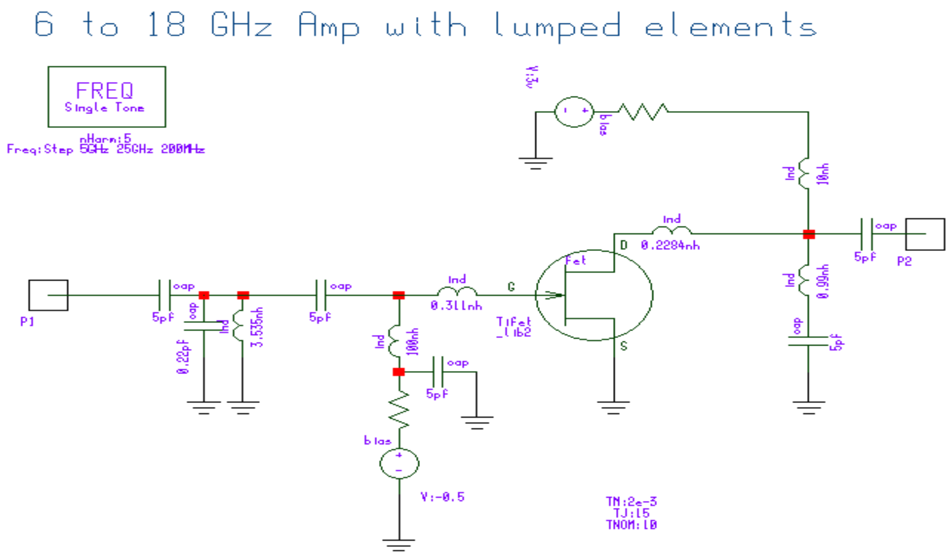

Figure 17: Schematic of the wideband amplifier with lumped elements

A first order validation is that for the given extracted SPICE type parameter the frequency response shown in Figure 18 by S11, S21 and S22; which, meets specification, with the standard model, which was modified for exact spot noise calculation. It shows that the amplifier has very flat gain (S21) as well as very good return loss (S11 and S22). First, we will consider what happens at room temperature.

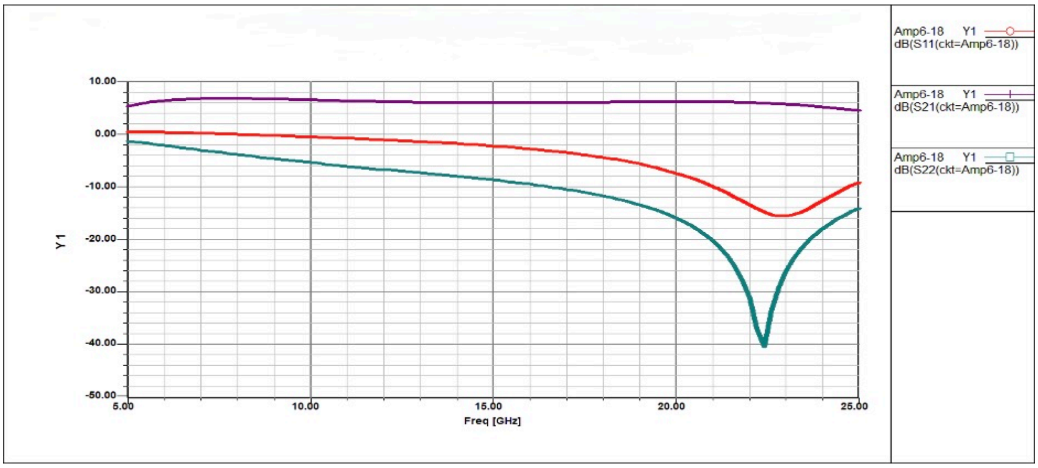

Figure 18: The amplifier exhibits very flat gain as well as very good input and output return loss

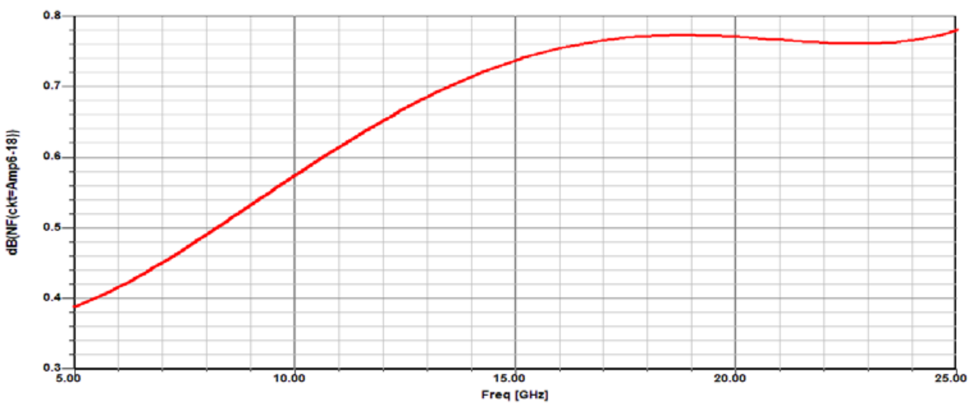

Figure 19: 50 Ohm noise figure.

Finally, the noise figure (i.e. 10log noise factor) varies from 0.38 to 0.78 dB over a frequency range of 5 GHz to 25GHz depicted in Figure 19. These extremely low values are due to the cooling. To proceed with design, it is not really possible to design an amplifier up to 20 GHz with lumped components due to the parasitic elements. Therefore, we must now switch, as expected, to design with distributed elements shown in Figure 20.

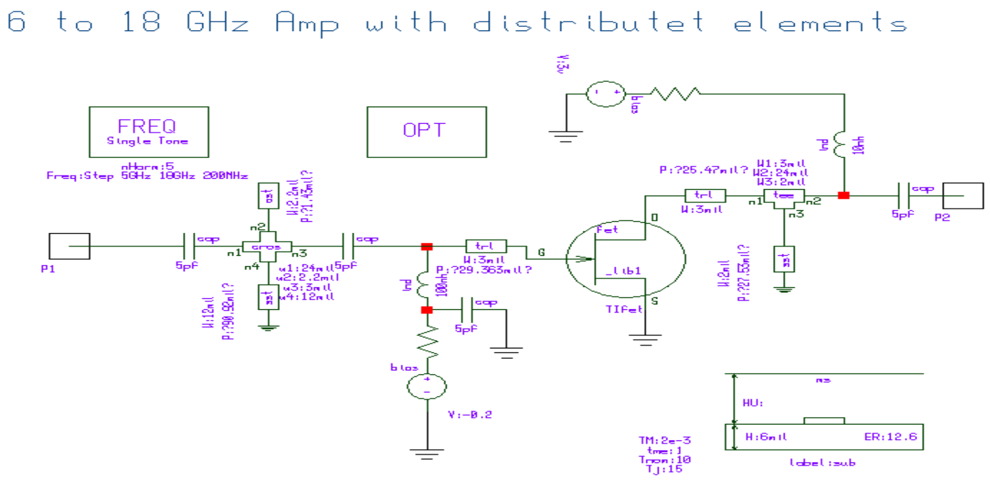

Figure 20: Wideband amplifier with lossy microwave distributed components, Tj=15k

Figure 21 shows the simulated frequency response of S11 S21 and S22 for the same amplifier but with distributed elements that can actually be fabricated in the real world. The Simulated noise figure is varies from 0.8dB to 1.5dB over a frequency range of 5GHz to 15GHz shown in Figure 22.

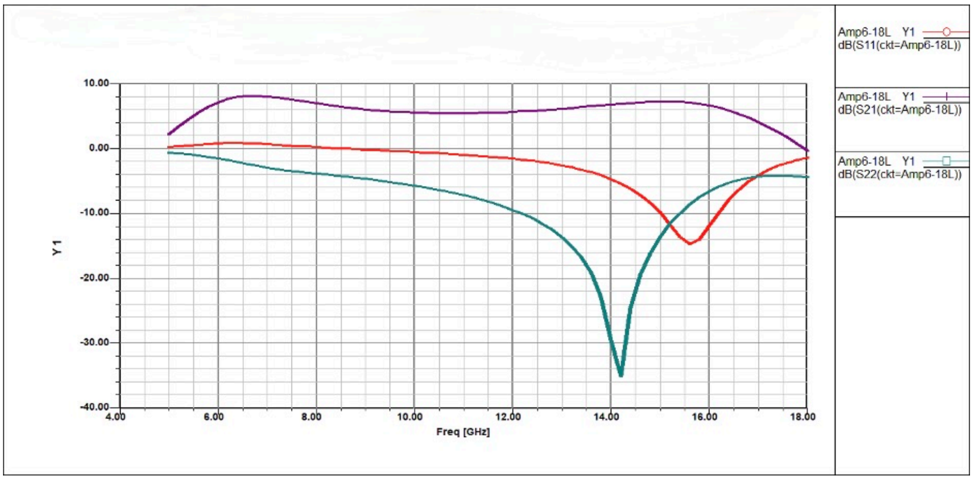

Figure 21: Frequency response for the same amplifier with distributed elements

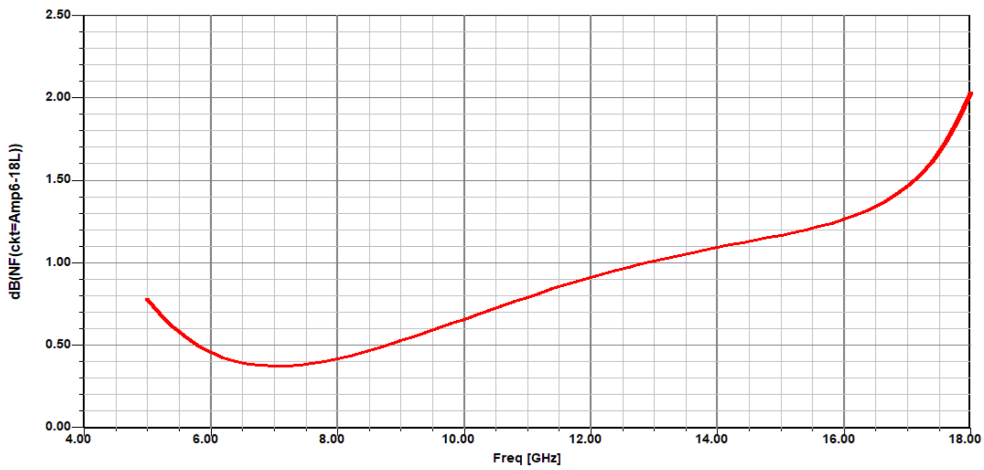

Figure 22: Degraded noise figure due to substrate losses in the distributed elements.

Because of substrate-induced losses in the distributed elements, the noise figure of this arrangement suffers greatly. We examine this factor here. For reference, most very low temperature transistor amplifiers are quoted in K (degrees Kelvin), rather than in noise figure. We can convert between noise figure and noise temperature as follows:

$$\text{Noise temperature (K)} = \mathrm{T_{REF}} * \left(10^{\frac{\mathrm{NF(dB)}}{10}} - 1\right) \tag{131}$$

$$\text{Noise figure (dB)} = 10 * \log 10 \left(\frac{T_{Noise}\,(K)}{T_{Ref}\,(K)} + 1\right) \tag{132}$$

Note that unless otherwise specified, $\mathrm{T_{Ref}} = 290$ K. The following table 4 results:

Table 4: Variation of noise figure with respect to noise temperature T_N (K) change

NF (dB)	T_N (K)	NF (dB)	T_N (K)
0.1	7	2.1	180
0.2	14	2.2	191
0.3	21	2.3	202
0.4	28	2.4	214
0.5	35	2.5	226
0.6	43	2.6	238
0.7	51	2.7	250
0.8	59	2.8	263
0.9	67	2.9	275

1.0	75	3.0	289
1.1	84	3.1	302
1.2	92	3.2	316
1.3	101	3.3	330
1.4	110	3.4	344
1.5	120	3.5	359
1.6	129	3.6	374
1.7	139	3.7	390
1.8	149	3.8	406
1.9	159	3.9	422
2.0	170	4.0	438

Therefore, the frequently quoted value of 17 K translates into a noise figure of 0.265 dB. However, it is very difficult to measure such a low value. (Note that some experts prefer to use the signal-to-noise (S/N) ratio to determine the noise figure.)

Figure 23 shows a validation circuit using a 14.7 K junction temperature and lossy distributed matching. This is based on [5]. The non-optimized gain of the circuit displayed in Figure 24. We can see that the non-optimized gain has clearly increased in comparison to lumped element matching network shown in Figure 18.

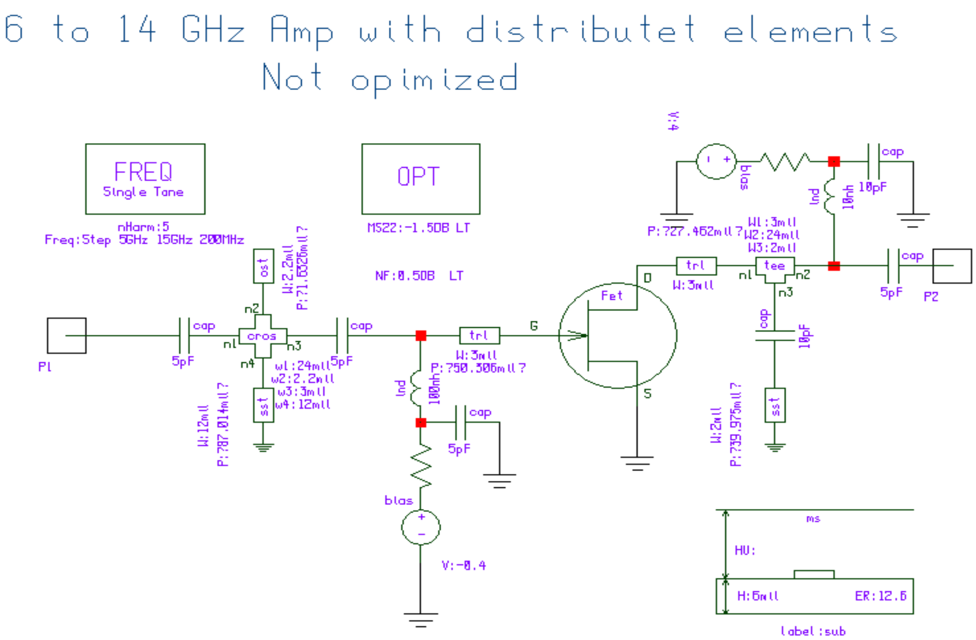

Figure 23: Experimental design for the low-temperature amplifier and lossy distributed elements

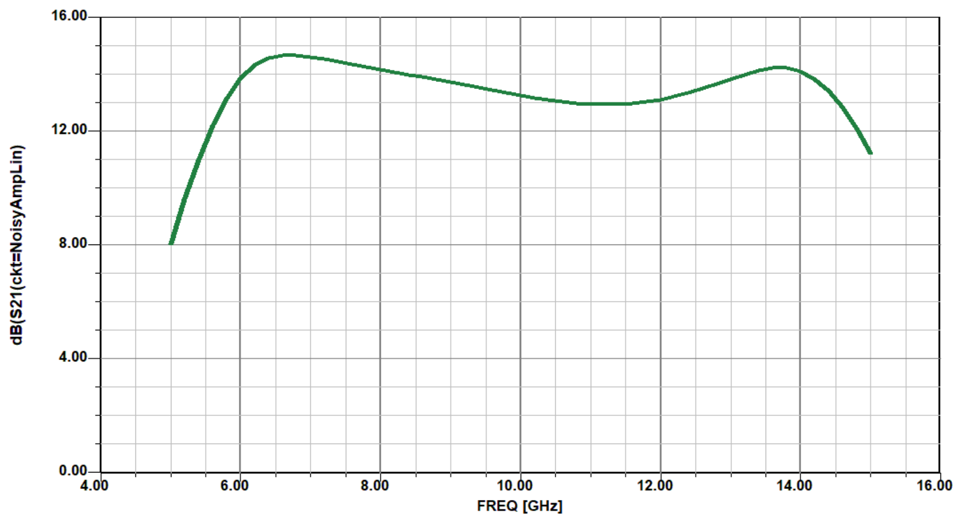

Figure 24: Significantly higher gain in the low-temperature amplifier

Figure 25 shows the simulated noise figure of the distributed element matching amplifier. The simulated Fmin is about 0.14 dB while NF is about 0.29dB from 5 GHz to 14 GHz. Although the noise figure is much improved, it is very tough to measure in the real world.

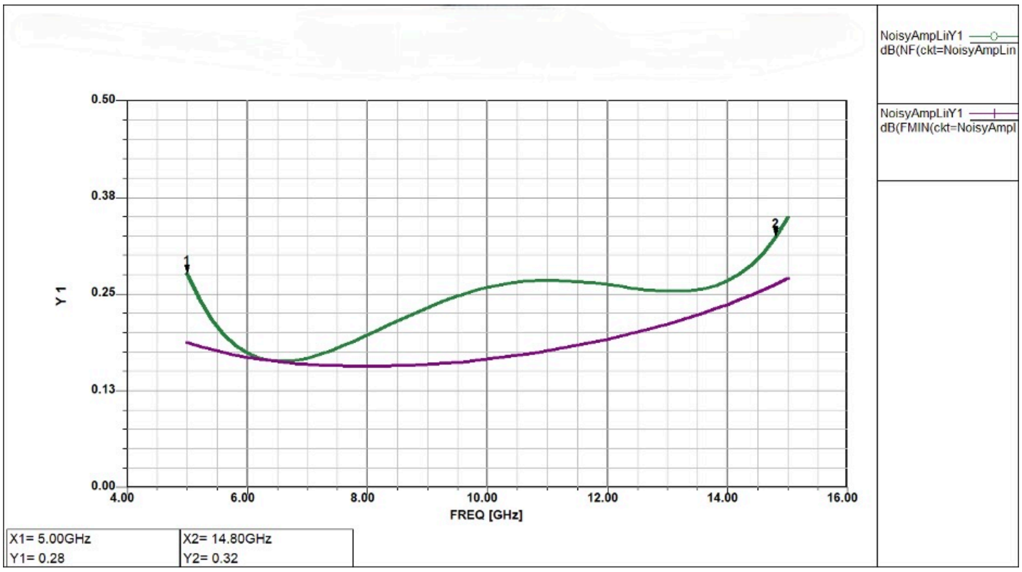

Figure 25: Simulated noise figure

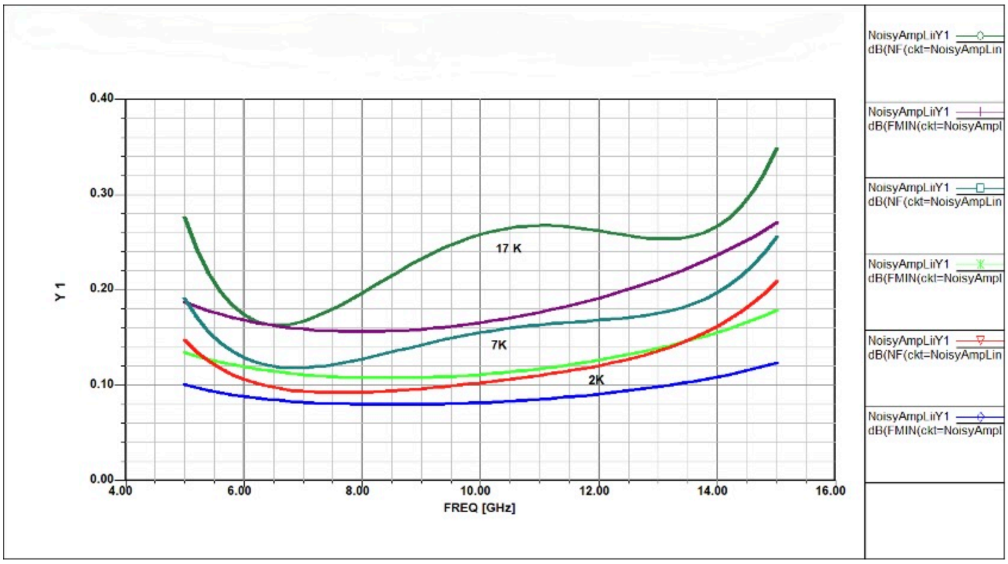

Figure 26: Simulated noise figure at different operating temperatures

Figure 26 shows the simulated noise figure at different operating temperatures in Kelvin (K). Since a temperature of 2 K corresponds to a noise figure of 0.08 dB, this is clearly "impossible" to measure!

3.1 Dynamic Range of the Amplifier

Now we will look at the three-tone dynamic range test which was popular for designing transistors in the cable TV (CATV) era. Since there are so many signals bombarding the antenna in the current state of play for satellite constellations in orbit and within view of the antenna system, a test with white noise as a test signal would be better, but it is hard to produce.

Examining previous practice in cable TV amplifier (CATV) design is useful. A commonly employed CATV test used a three tone test, comprised of an FM channel with two sidebands. The modulation index for HiFi (High-Fidelity) was selected to be 5, the upper audio frequency is 16 kHz. Thus, the bandwidth/sideband =16 x 5 = 80 kHz, or 160 kHz total bandwidth.

Analog video bandwidth:

NTSC: The NTSC (National Television System Committee) standard, a common analog TV format, uses a 6 MHz bandwidth for each channel, with the video signal occupying the first 4 MHz.

Luminance (Y): The luminance signal, which carries the black and white information, has a bandwidth of 4.2 MHz.

Chrominance (Color): The chrominance signals (I and Q) carry color information and have lower bandwidths (1.6 MHz for I, 0.6 MHz for Q) because the human eye is less sensitive to color details than to brightness.

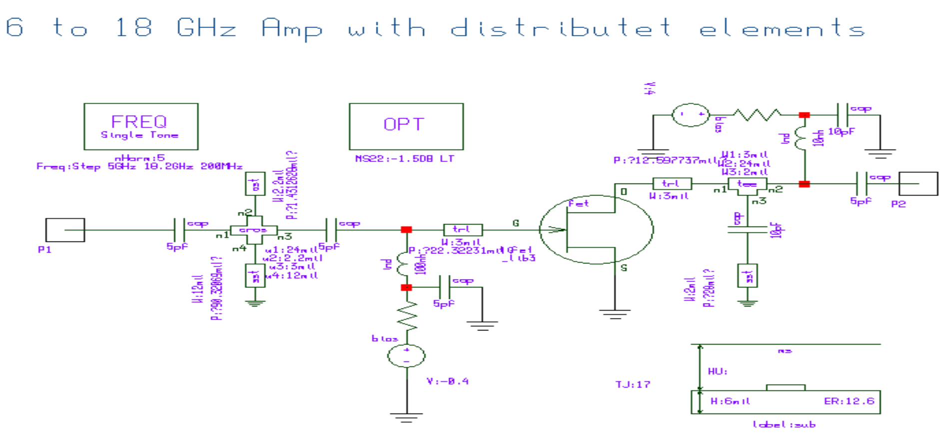

Figure 27: Experimental circuit for large-signal operation at room temperature

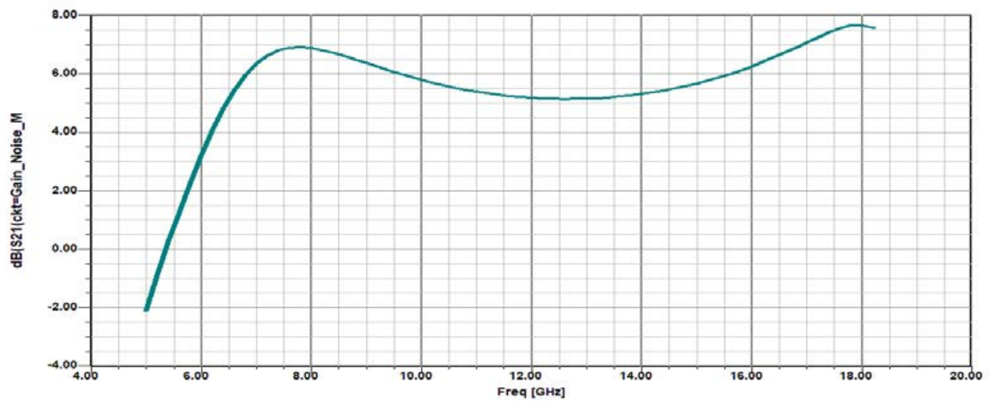

Figure 28: Frequency response at the bias level as seen in Figure 27

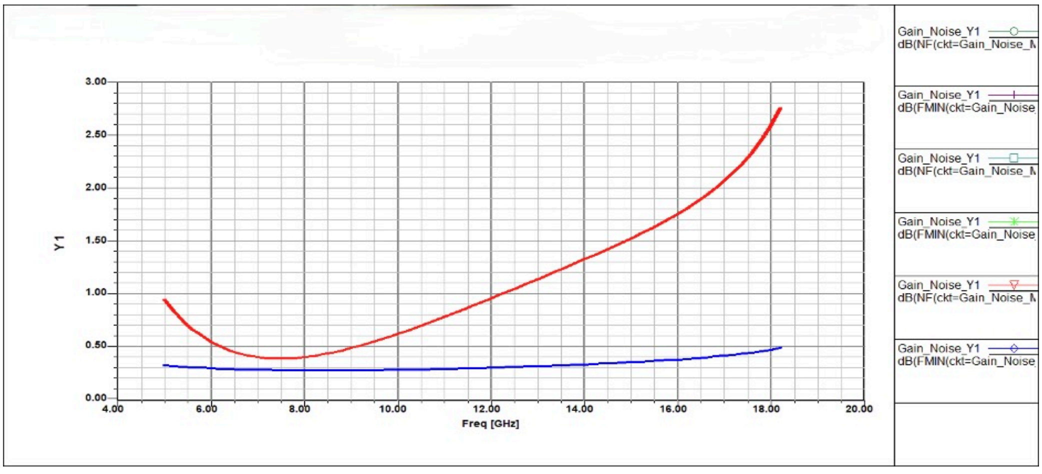

Figure 29: Noise figure at the bias level as seen in Figure 27, see: blue=Fmin, red = predicted NF

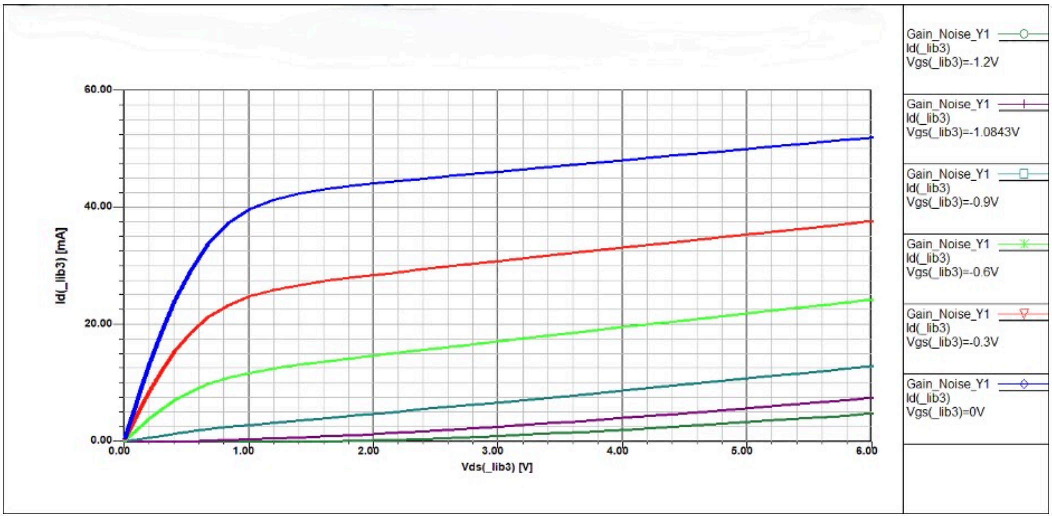

Figure 30: Simulated DC current–voltage (I–V) curve for the amplifier

From a previous Raytheon–TI joint venture, we had some Materka model parameters that we adjusted to fit the values of the GaN transistor that were published in [4, for further details, see p.p. 705 (AlGaN/GaN HEMT)]. This involved changing the intrinsic capacitance values and some other parameters to emulate this device. The actual frequency response did not change much.

While the two-tone test is usually recommended, as we explained the three-tone test comes closer to the practical multitoned environment.

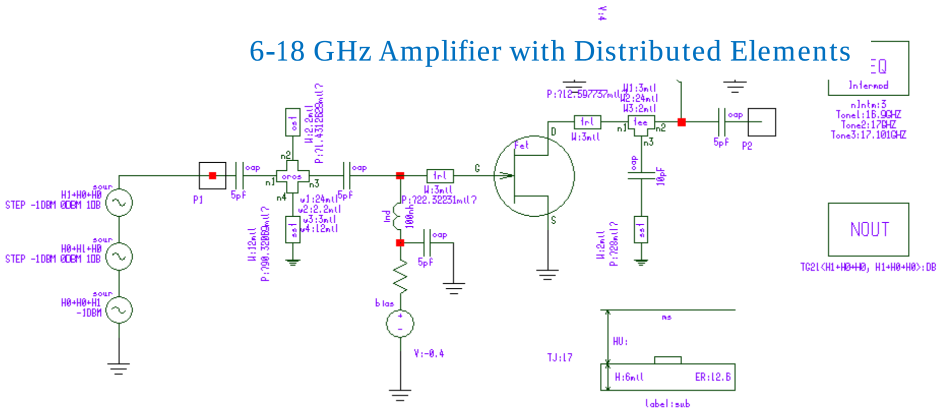

Figure 31: 6 to 18 GHz amplifier with distributed elements (experimental circuit for operation with larger signals)

Note especially the three-tone input in the circuit for operation with larger signals.

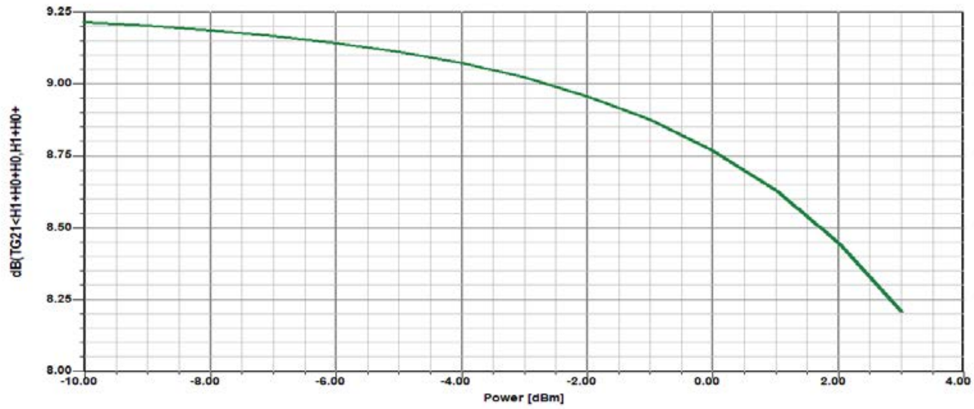

Figure 32: Three-tone output (power sweep)

As shown in the simulated linearity test in Figure 32, it is important to determine the 1 dB compression point. It occurs at about 3 dBm output or –5.2 dBm input. As long as the model has a good fit, this is an ideal parameter to examine. The Figure 33 shows power load lines as function of gate voltage sweeping from 0 to 1.2V. In fact it is a tune circuit shows elliptical plot instead of a purely resistive which is straight line. The load line indicates stored energy (fly wheel effect).

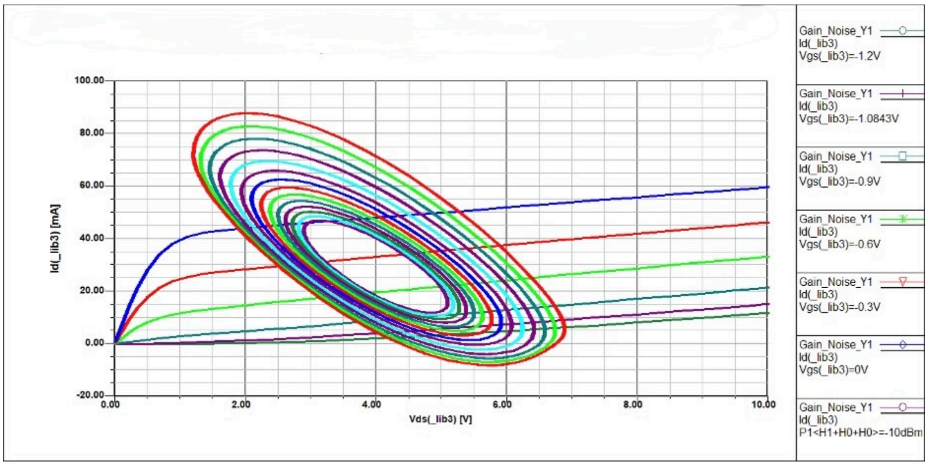

Figure 33: Simulated output power load lines

The simulated output power load lines show the power compression very nicely in Figure 33.

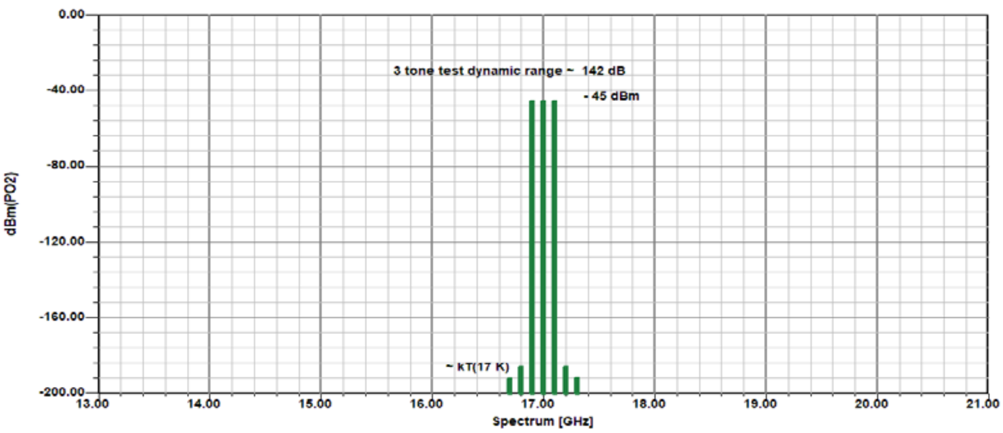

Figure 34: Predicted dynamic range at 10 GHz and three-tone test of about 3 x 1mV rms

The simulated dynamic range of this circuit, shown in Figure 34, is about 142 dB relative to -45 dBm input power, which is impressive. (The textbook three-tone test would have one tone smaller by 6 dB.)

Now we will look at a 90 GHz amplifier designed for a temperature of 10 K shown in Figure 35. It consists of a CFY99A experimental transistor, uses ideal transmission lines. Figure 36 and Figure 37 shows the simulated gain (S21) and output return loss (S22) at 10 K and Simulated noise figure respectively.

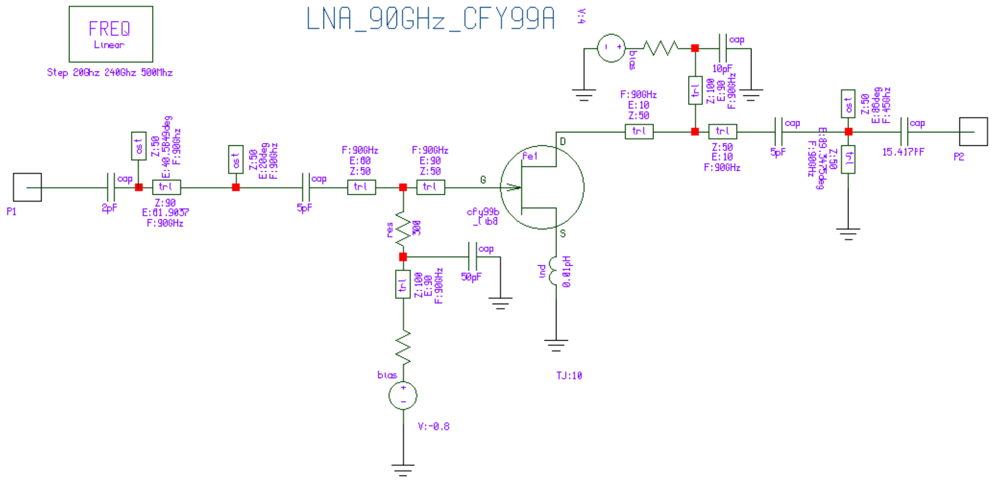

Figure 35: Cooled amplifier (low-noise 90 GHz amplifier using ideal distributed elements)

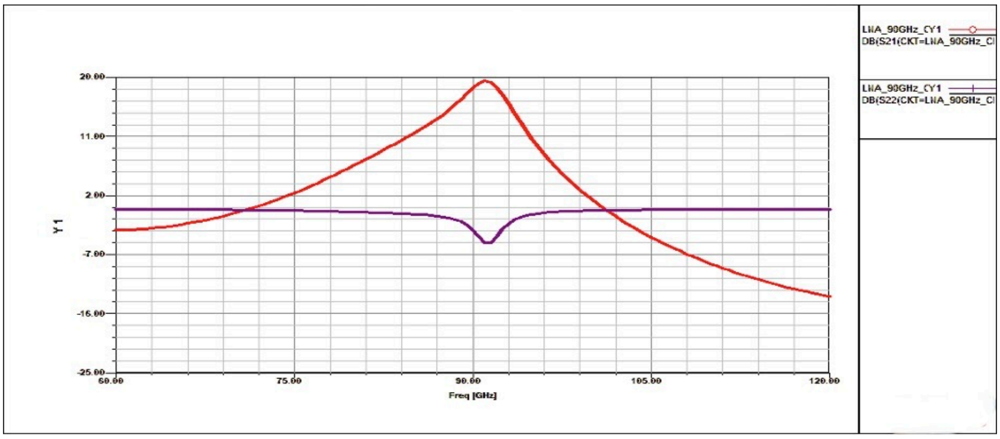

Figure 36: Simulated gain (S21) and output return loss (S22) at 10 K

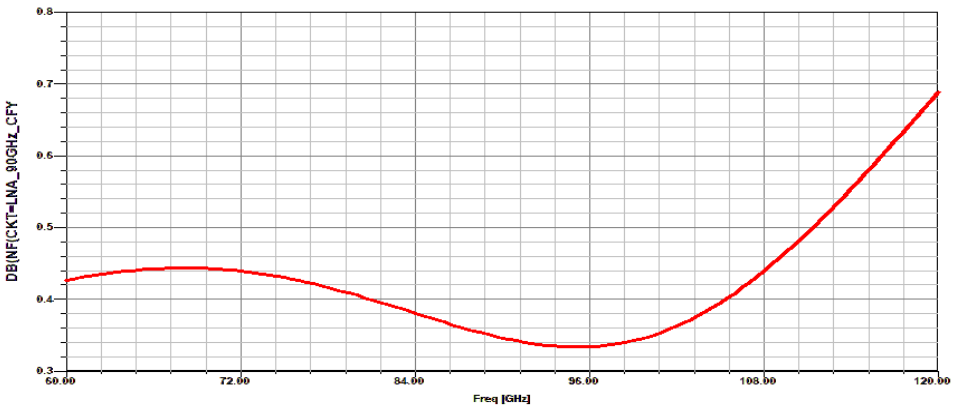

Figure 37: Simulated noise figure for the same amplifier

3.2 Reverse-Engineered Two-Stage Amplifier

Now we will consider an experiment involving the reverse engineering of a two-stage amplifier. The amplifier in question is described in [3]. We have two stage amplifier working in range of from 80 to 100GHz. It has proper input, output and proper inter-stage matching. The gain S21 (dB) is pretty flat from 80GHz to 105GHz, (good design approach). As can be seen from Figure 39 S11 (dB) and S22 (dB) the amplifier is unconditionally stable.

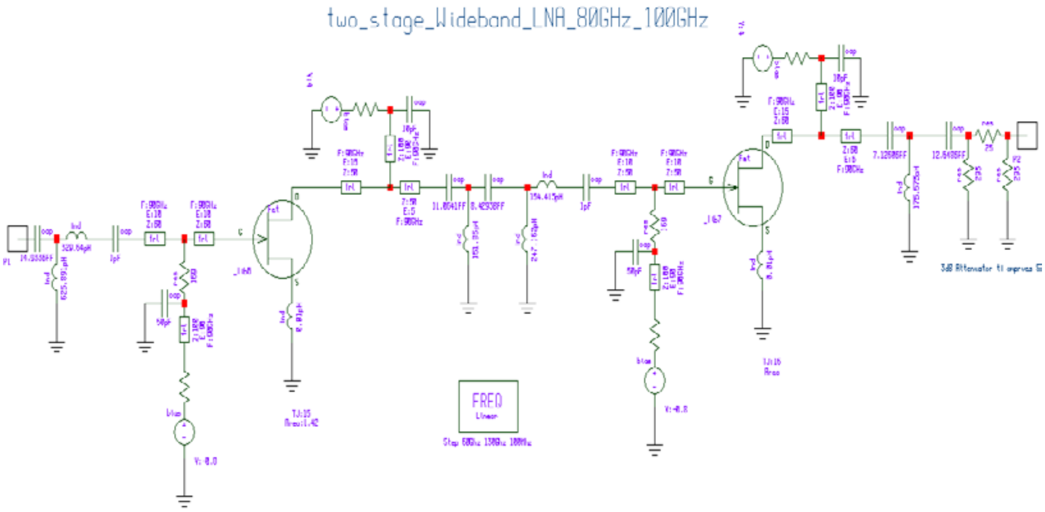

Figure 38: Circuit diagram of the two-stage amplifier as published in [3]

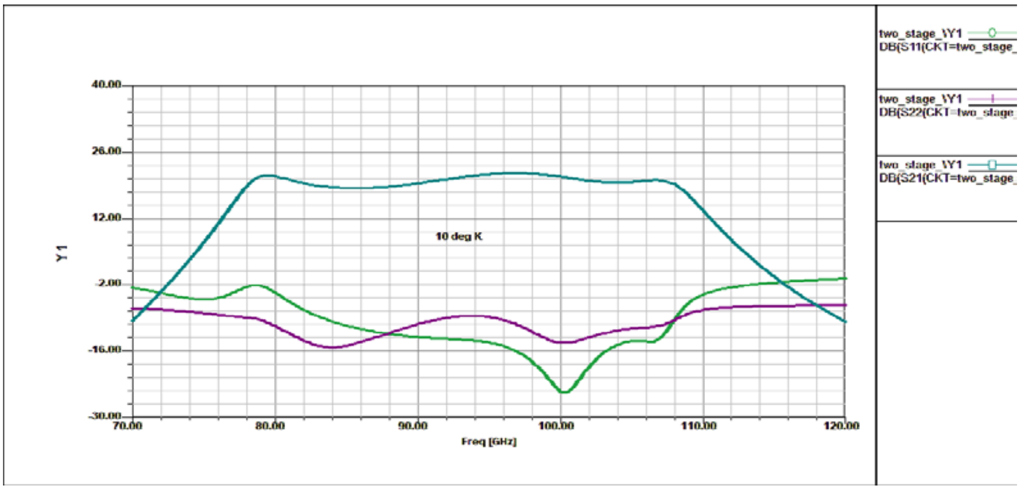

Figure 39: Simulation of the gain and return loss of the 100 GHz amplifier described above

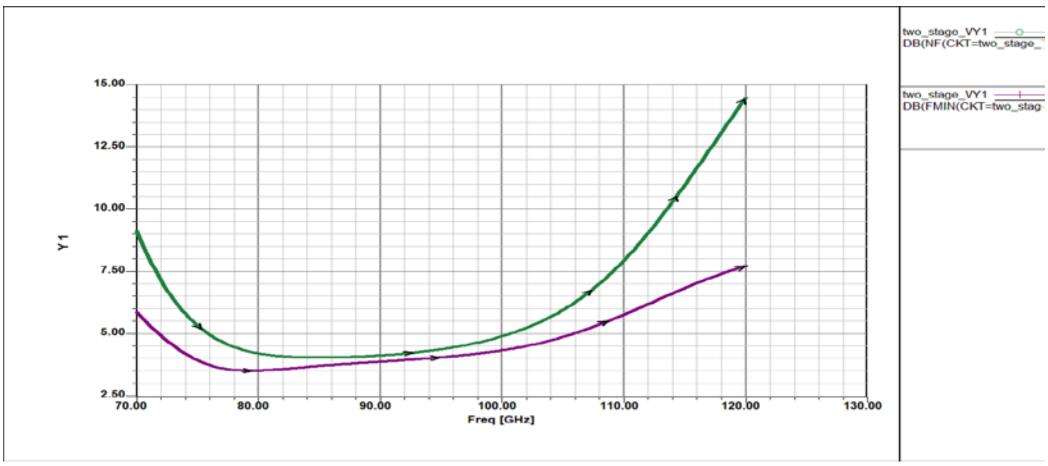

Figure 40: Noise simulation at 300 K

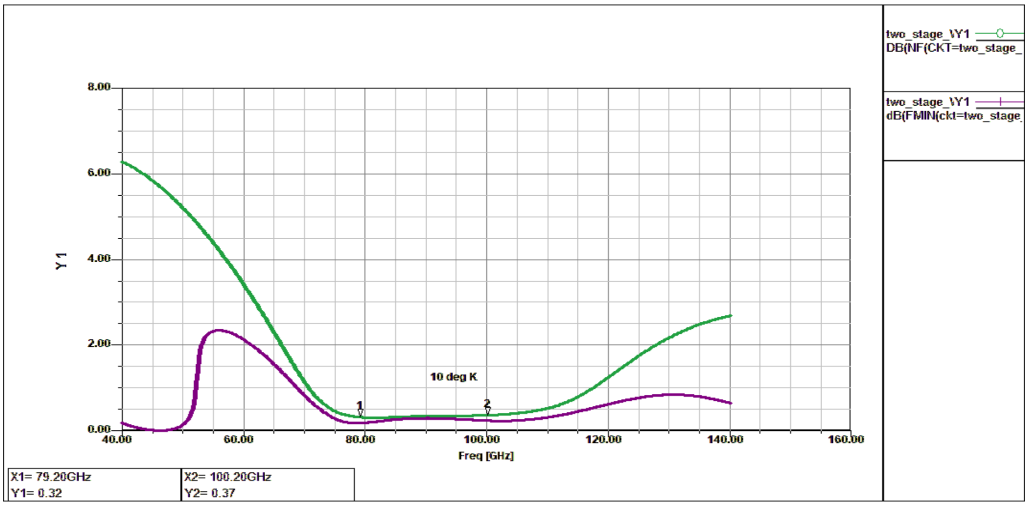

Figure 41: Noise simulation at 10 deg K after optimization.

The Figure 41 shows the simulated noise figure when the circuit is cooled down to 10 deg K. The circuit simulated noise figure in a 50 ohm system and minimum noise figure is about 0.33 dB avg. from 80GHz to 100GHz.

One of the limitations is that, because of the required high dynamic range of this types of amplifiers, the FET cannot be operated at minimum noise figure at 20% of Idss, but slightly higher. Therefore operating noise figure is slightly worst. Also, the thermal conductivity from the device to the ground needs to be improved in future work (GaN).

Overall Summary of This Paper

We have presented a detailed discussion of cryogenic amplifier performance, comparing with published data model expressions. Our results show that modern CAD simulators, with advanced noise models built in, can accurately predict core transistor performance compared to expectations from mathematical performance models, including gain and matching. These simulators are also able to predict the available dynamic range of the amplifier, from minimal discernable signal to the 1 dB compression point. In the case chosen here, the simulated dynamic range is 142 dB/Sqrt(B), where B=1 Hz for the rarely used 3 tone test. As mentioned previously, in the modern era with large numbers of satellites bombarding antennas with large signals, the question of dynamic range becomes a pressing design issue. This study's results provide a foundation for future designs achieving superior dynamic range while preserving excellent noise performance.

We conclude with comments taken from [42], "The GaN-HEMTs offer a unique combination of low-noise and high-power handling capabilities. This feature is expected being increasingly requested by modern low-noise applications, including those operating at cryogenic temperatures and RFI environments. The relatively larger power dissipation, compared to other technologies, is one of the main challenges facing the GaN HEMTs for low-noise applications. Nevertheless, the technological development of the GaN-HEMTs is increasingly shortening the gap with other more established technologies which took advantage from their earlier development. These advances are due to an aggressive lateral scaling of the device, the optimization of the vertical epitaxy as well as that of the ohmic and Schottky contacts. The impact of these improvements at cryogenic temperatures are still to be demonstrated in the future."

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